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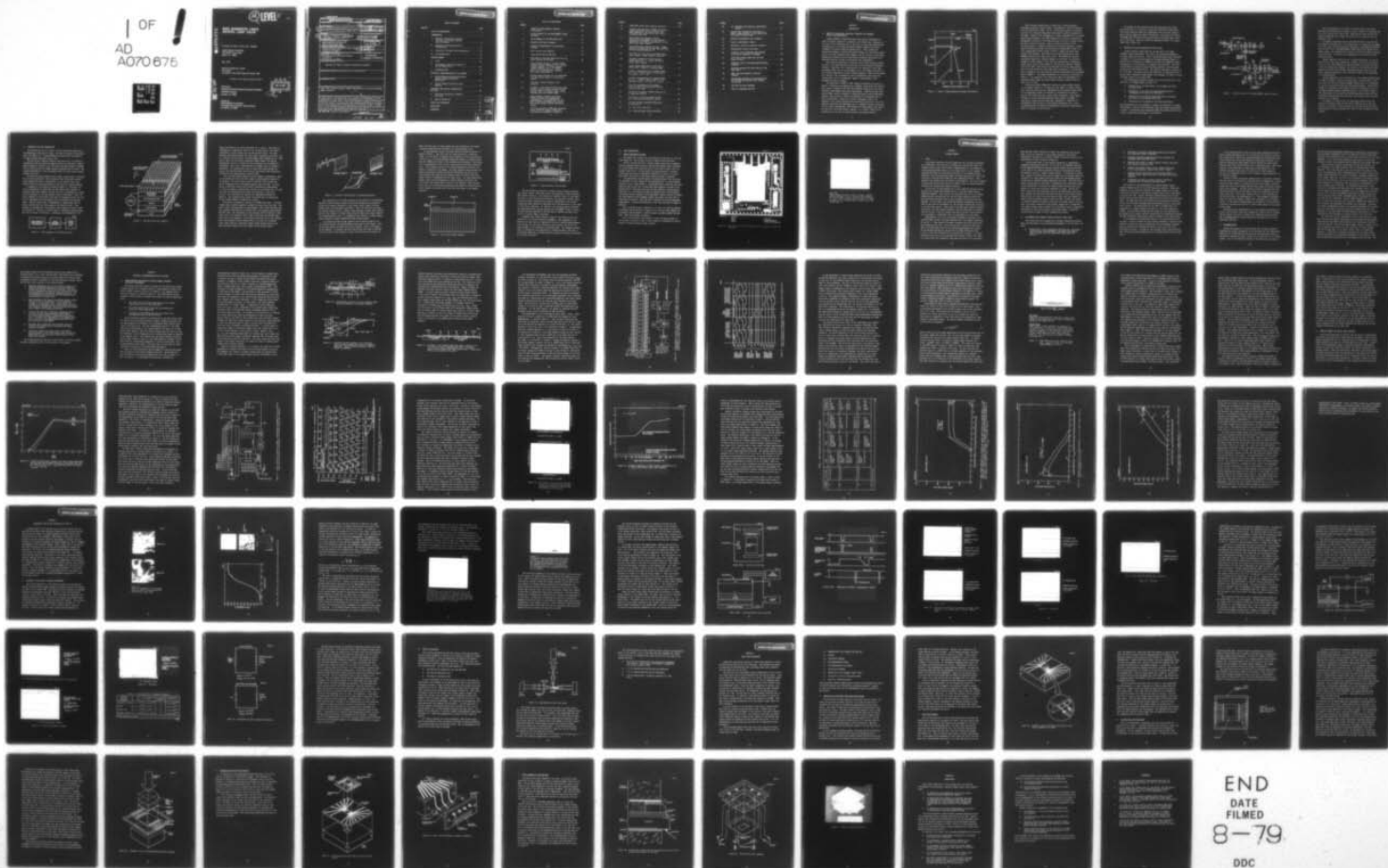
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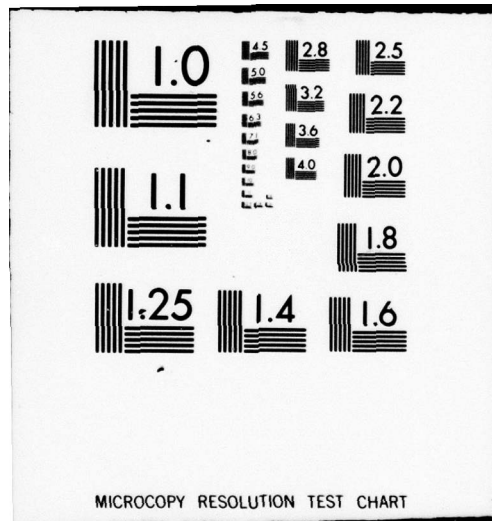
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WIDE BANDWIDTH LIQUID CRYSTAL LIGHT VALVE

P. Braatz, M. Little, V. Efron, and J. Grinberg

Hughes Research Laboratories
3011 Malibu Canyon Road
Malibu, CA 90265

May 1979

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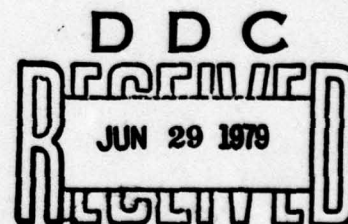
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During this contract, we accomplished the following major tasks toward the development of a CCD liquid-crystal light valve. We have demonstrated a fully operational CCD LCLV with a contrast ratio of 50:1 and a spatial resolution of 12 lines across the device. An alternative chip dicing method has been developed that reduces degradation to the substrate by a factor of 100. In addition, a new CCD LCLV packaging technique has been developed that improves the light valve fabrication yield from 30% to 80%.		

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SECTION 1

INTRODUCTION

A. NEED FOR A REAL-TIME, PRACTICAL INTERFACE FOR COHERENT OPTICAL DATA PROCESSING

Recent advances in microelectronics have greatly increased the power of digital computers to calculate and process data. However, in the face of the increasing need to be able to process two-dimensionally organized data, the present electronic digital computer has proven inadequate in several important applications. These include the machine processing of pictures and sensor images, the real-time processing of very wide bandwidth radar signals, and the solution of the multi-dimensional nonlinear partial differential equations that govern such important physical systems as meteorology and aerodynamics.

The potential advantage of coherent optical data processing (CODP) is that it can simultaneously process data on many parallel processing channels. Therefore, this technology has the potential of very high processing speed, and it is considered to be a promising alternative to the serially organized electronic digital computer. CODP is particularly well suited to the processing of the two-dimensional data bases mentioned above, such as photographic images or multichannel, wide-bandwidth electronic signals.

The importance of CODP to radar signal processing is indicated in Figure 1 (prepared by Bob Markevitch of Ampex), which shows the approximate range of bandwidth (BW) and time bandwidth product for four quite different radar-signal-processing technologies. High BW and time bandwidth product values correspond to higher-resolution radar performance. Clearly, CODP provides a range of performance far surpassing that of other technologies. Despite its obvious advantages, CODP is not regarded to be a general-purpose data-processing technology. Since the physical components and subsystems used to implement optical processing are not easily programmable, CODP systems are substantially less flexible than the electronic digital computer. As a result, CODP is best implemented in the form of special-purpose processing hardware.

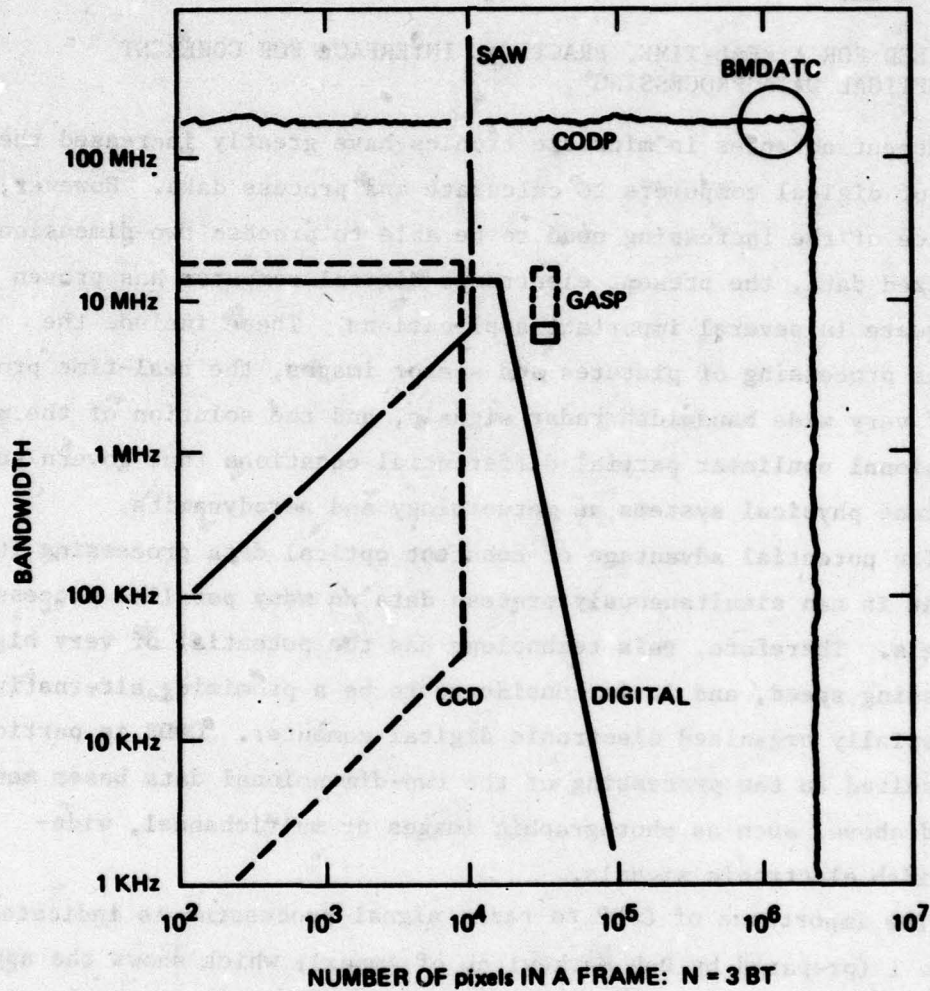


Figure 1. Limits of radar-signal-processing technologies.

There are many problem areas in which such a special-purpose processing capability could be used. Unfortunately, few have benefited from the potentials of CODP. One of the principal reasons, we believe, is a lack of a practical high-speed electrical-to-optical transducer at the input. Speed of data throughput is a basic requirement for a special-purpose data processor. Yet CODP, because of its historic reliance on photographic film both for entering data and for use as a spatial filter, has been an off-line process. Thus it suffers the worst of both processing worlds — limited flexibility and off-line operation. Hughes Research Laboratories (HRL) has developed for NASA/Goddard (under contract numbers NAS 5-23192 and NAS 5-22413) a unique new device that resolves this dilemma. This device is the hybrid field-effect mode (HYFEM) liquid-crystal light valve (LCLV). The HYFEM LCLV converts noncoherent images into coherent images, in real time. The device is designed to input images in real time from noncoherently illuminated scenes and to convert these images to the spatially coherent illumination of the CODP. This device is being used for various applications, and it has been tested for fast radar data processing in a system being built by Ampex for the Army Ballistic Missile Defense Advanced Technology Center (BMDATC). The design performance of the system is indicated in Figure 1. For comparison, the figure also shows the performance of a government/Ampex signal processor (GASP) in which a General Electric light valve is used.

The photoactivated HYFEM LCLV requires an input primary display. If the primary display is a cathode ray tube (CRT) or a laser scanner, then resolution and speed are compromised and the system becomes bulky. In the Ampex/Army system, the scanning is performed by an acousto-optical (AO) delay line and a pulsed laser illuminator. This system, although it can process high-frequency radar signals (150 MHz), is complicated, large, and has high power consumption. Therefore, it accomplishes only one part of the required performance (i.e., high processing speed) and cannot be implemented in practical applications. Thus, it is merely a test vehicle.

The purpose of the charge-coupled device/liquid-crystal light valve (CCD LCLV) is to serve as a practical solid-state input device. This device should be small and lightweight, have low power requirements, and be rugged and simple in operation. The device will combine the HYFEM LCLV (the same as the photoactivated thin-film light valve) with a CCD array. This will yield the additional benefit of an eight times faster frame rate.

B. EXAMPLES OF DOD APPLICATIONS OF THE CCD LCLV

A major potential application of the CCD LCLV is for high-bandwidth signal processing. The task is the precise determination of target range and velocity. Such a system (mentioned above and shown in Figure 2) is now being developed by the Ampex Research Center in Redwood City, California, for BMDATC on Contract No. DASG60-77-C-0010. The modulator in this system is the Hughes thin-film LCLV. The first LCLV performs an initial matched filtering operation, and the second provides the final CODP function. The system is designed to operate at up to 150 MHz. The system uses an AO delay line in conjunction with a pulsed laser illuminator (mode-locked, cavity-dumped ion laser) to write the radar signal on the second LCLV.

The configuration changes in going from the thin-film LCLV to the CCD LCLV in the BMDATC/Ampex processor are

- Elimination of the mode-locked, cavity-dumped ion laser for data input.
- Elimination of the precision imaging/scanning optics (including two AO cells) for data input.
- Elimination of the CRT and associated drive electronics and optics for correlation mask input.
- Elimination of the geometric correction subsystems.

These components are very expensive, complex, and difficult to operate and maintain. They are also physically large and consume large amounts of power. Eliminating these components makes the system practical and allows a significant improvement in performance.

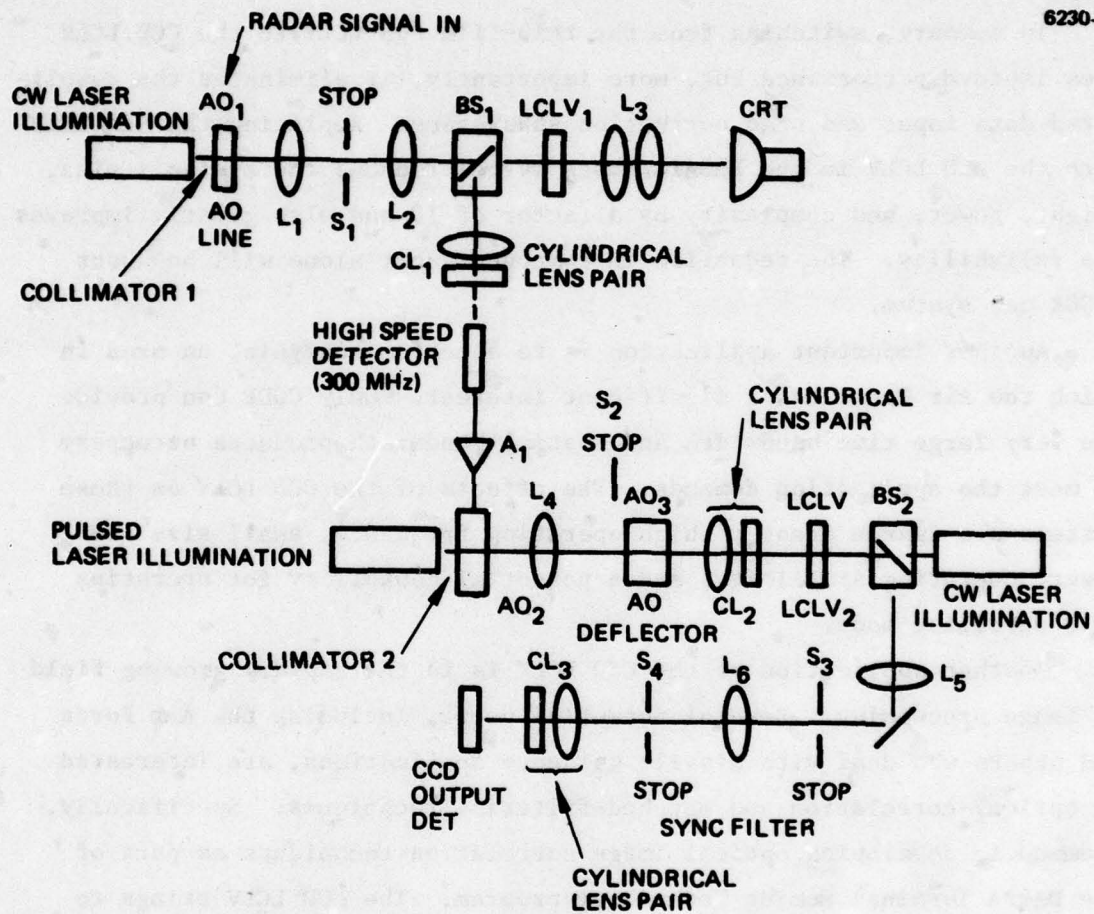


Figure 2. Optical system for the Ampex/BMDATC signal processor.

The CdS photosensor in the LCLV is characterized by slow decay. Therefore, the system shown in Figure 2 will be capable of operating only at a very low duty cycle ratio (2%). Replacing the slow CdS with fast silicon substrates will increase the duty cycle by almost an order of magnitude (8X).

In summary, switching from the thin-film CdS LCLV to the CCD LCLV does improve performance but, more importantly, it eliminates the complicated data input and scan correction subsystems. Replacing the CdS LCLV with the CCD LCLV in the BMDATC/Ampex system reduces the system's size, weight, power, and complexity by a factor of 10 and also greatly improves its reliability. The reduction in component cost alone will be about \$100K per system.

Another important application is to spectrum analysis, an area in which the Air Force has a significant interest. Only CODP can provide the very large time bandwidth and spatial bandwidth products necessary to meet the application demands. The effects of the CCD LCLV on these systems are in the areas of high operating frequency, small size and power, operating simplicity, and a potential capability for operating in a scrolling mode.

Another application of the CCD LCLV is in the rapidly growing field of image processing. Several potential users, including the Air Force and others who deal with missile guidance applications, are interested in optical-correlation and matched-filtering techniques. Specifically, Grumman is developing optical image correlation techniques as part of the DARPA Terminal Homing Technology program. The CCD LCLV brings to this application all the positive features mentioned earlier and also practically absolute position definition and stability, which is quite important to the system.

In summary, we believe that the long-range simplification and stability realizable using the CCD LCLV in CODP systems is the real benefit of the device. These features and the high system effectiveness provided by high performance will lead to user acceptance of CODP systems.

C. CONCEPTUAL CCD LCLV DESCRIPTION

The CCD LCLV driver can convert a serial electrical signal into a two-dimensional (2-D) optical image. The device consists of three main parts (see Figure 3): a high-bandwidth serial/parallel CCD register, an image transfer mechanism, and an LCLV.

The CCD circuit converts serially coded data into a 2-D frame of information, which is stored as charge packets in a CCD array. When an enable command is applied to the CCD array, the whole frame of information is transferred by the image transfer mechanism into the LCLV. The transfer mechanism is a fully integrated (with the CCD) silicon charge-transfer structure.

The electric field produced by the signal charge causes a reorientation of the LC molecules. This rotation of the birefringent LC molecules changes the plane of polarization of the read-out beam. This change in state of the polarization is then read out with an analyzer.

A schematic of the device is shown in Figure 4. Initially, one line of information is loaded into the CCD serial input register (x register). When this register is full, the line of information is transferred in parallel to the CCD parallel array (y direction). Next, the serial register is filled with a new line of information while the first line of information is being shifted one step upward in the parallel array. Then the second line of information is transferred from the serial register into the first stage of the parallel array. This sequence is repeated until the parallel array contains an entire frame of information. Finally, the whole frame is transferred simultaneously into the LV layers (z direction). Therefore, the information in the

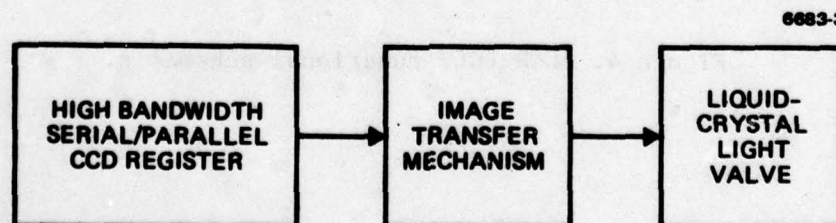


Figure 3. Block diagram of the CCD-driven LCLV.

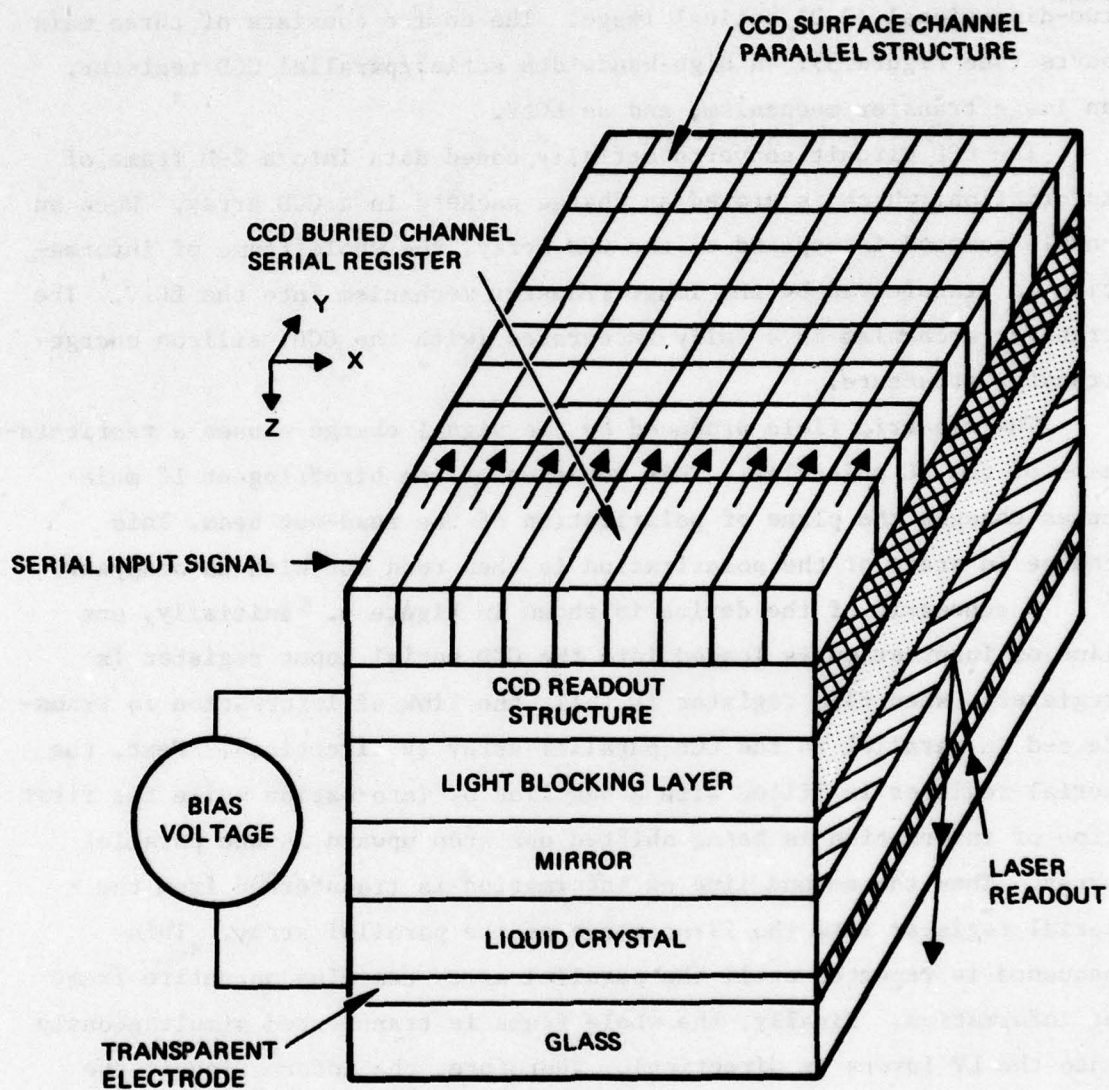


Figure 4. CCD/LCLV functional schematic.

device has moved in all three directions (x, y, and z). The frame of information is temporarily stored in the LC layer while a new frame of information is being loaded into the CCD parallel array. The laser read-out beam passes through the front glass, transparent electrode, and LC, reflects from the mirror, and then passes again through the LC. When the LC layer is activated by sufficient signal charge, the optical polarization vector is rotated in direct proportion to the degree of activation. This can be converted with an analyzer into an intensity modulation. By absorbing any read-out light that leaks through the mirror, the light-blocking layer protects the silicon from being photo-activated by the high-intensity read-out beam.

Since all ODP methods operate on whole frames of information, there is the prerequisite that the whole image be simultaneously present on the display. The input device, which is usually a CRT, accepts the serial information and is activated serially pixel by pixel. To use a CRT as an ODP input device would involve contradictory requirements: (1) that the image be simultaneously present at the display and (2) that the frame of information decay before the writing of a new one is started. This contradiction requires the compromise presented in Figure 5. The intensity decay across the screen must be significant if the residual image is required to be small.

The device is required to operate at 100 MHz data rates. A buried-channel type of serial register is needed to accept this data rate. This type of CCD is characterized by high-frequency clock rates (250 MHz) and high transfer efficiencies but suffers from a low charge-storage density per unit area. The information in the parallel array is shifted at much lower rates. For instance, with a 1000 x 1000 array and 100 MHz input rates, the clock frequency in the parallel section will be only 100 kHz. This result permits surface-channel CCDs to be used in the parallel array; these CCDs have inherently larger charge storage capacity and will therefore maximize the drive signal to the liquid crystal.

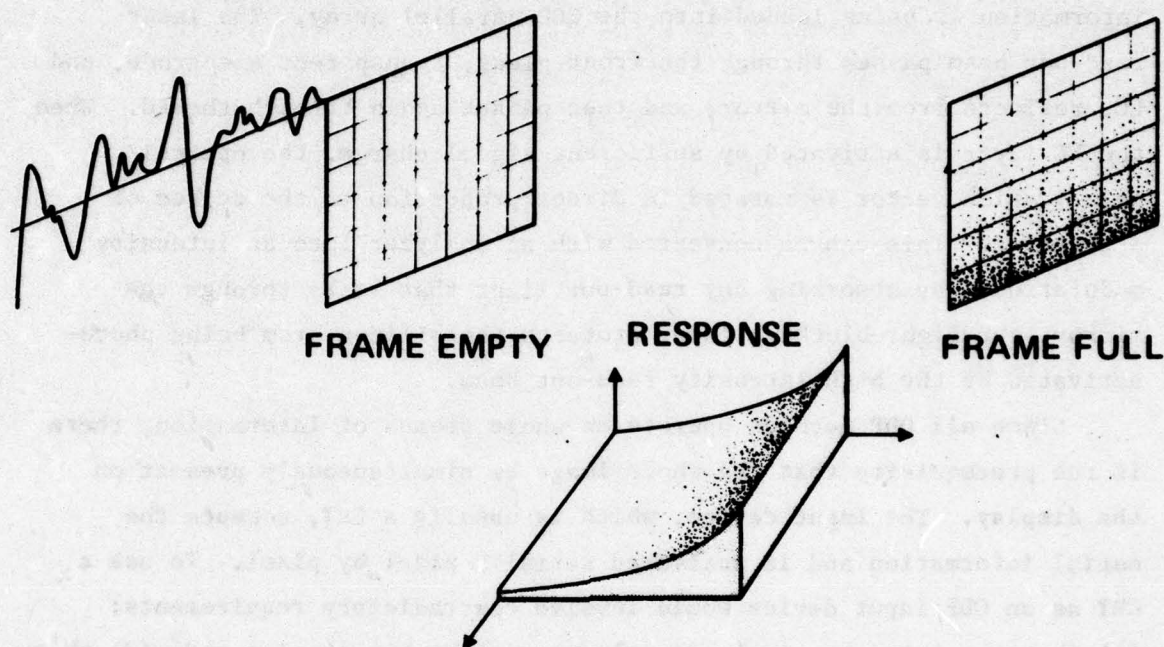


Figure 5. Intensity nonuniformity for nonstorage devices.

More importantly, the scheme utilized in this device for transferring spatially resolved signal charge from the CCD storage array through the almost fully depleted substrate to the liquid crystal cannot be accomplished from a buried-channel CCD (BCCD). Thus, the parallel array must use surface channel devices (SCCDs), which presents a rather novel requirement for the transfer of signal charge from the BCCD serial input register to the SCCD parallel array. To accomplish this transfer of signal charge, three alternative unique schemes have been devised by HRL.

To achieve the same storage capacity in the buried channel as in the surface channel, the buried-channel cells must be much longer. This can be done because the BCCD serial input register cells do not appear on the display. To minimize the dead time between the lines of information, the serial input register is split into two parts (see Figure 6).

While the first part is being loaded with the information, the second is being transferred from the BCCD to the SCCD parallel array.

A cross-sectional view of the basic CCD LCLV readout structure is shown in Figure 7. The thin ($125\text{ }\mu\text{m}$), high-resistivity π substrate ($1000 \leq \rho_s \leq 10\text{ k}\Omega\text{-cm}$) is normally fully depleted to the low-resistivity ($1\text{ }\Omega\text{-cm} \leq \rho_{\text{epi}} \leq 50\text{ }\Omega\text{-cm}$) epilayer during the transfer of signal charge from the CCD parallel array to the liquid-crystal interface. This transfer is accomplished by the electric field associated with the depletion layer. The orthogonal nature of the field distribution preserves the spatial resolution of the signal. The thin epitaxial layer provides the moderate-resistivity silicon on which is fabricated the surface and buried-channel CCD input and the storage arrays with which electrical signal charge is introduced into the light valve. The high-conductivity channel stops function primarily to isolate adjacent CCD lines, but since these also provide Ohmic contact to the epilayer, this structure can be used as an electrical ground plane with which to shield the electrical signals on the CCD side of the chip from those of the readout structure.

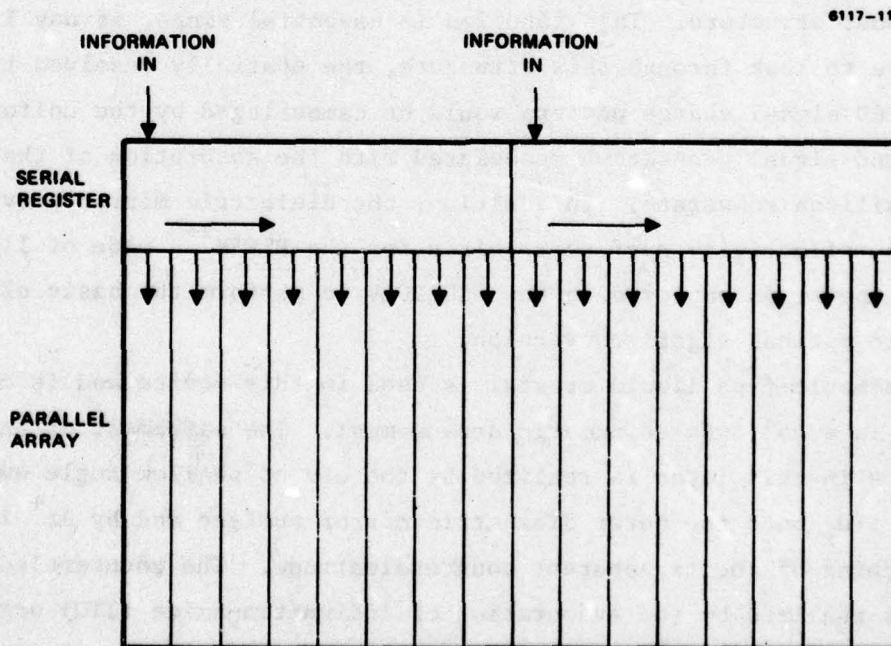


Figure 6. Split serial input register.

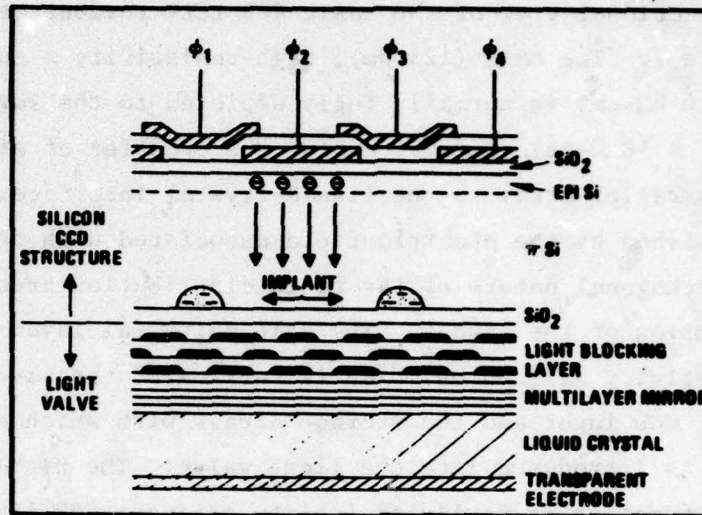


Figure 7. Cross section of the CCD LCLV.

The LBL and DM are intended to provide optical isolation between the intense readout light beam and the photosensitive, high-resistivity MOS readout structure. This function is essential since, if any light were able to leak through this structure, the spatially resolved transferred CCD signal charge pattern would be camouflaged by the uniform background signal generation associated with the absorption of that light in the silicon substrate. In addition, the dielectric mirror provides the high-reflectivity surface required for the HYFEM¹⁻³ mode of liquid-crystal operation employed in the CCD LCLV to perform the basic electrical to optical signal conversion.

A nematic-type liquid crystal is used in this device and is configured in a 45° twisted nematic arrangement. The alignment of the molecules in this layer is realized by the use of shallow angle evaporation of SiO_x onto the outer dielectric mirror surface and by Ar^+ ion beam etching of the transparent counterelectrode. The counterelectrode, which is realized by the evaporation of indium/tin-oxide (ITO) onto a thick glass substrate, provides mechanical support and optical uniformity for the whole CCD LCLV.

D. CHIP ORGANIZATION

1. Device Structures on Chip

Four main test circuits were included on the CCD side of this chip (see Figure 8). The purpose of each is briefly described below.

The 64 x 64 SPS array has a buried channel input serial register, surface channel parallel section, and surface channel output registers. It is the primary test structure and is to be used to make a 64 x 64 element light valve. In this array, the buried-channel to surface-channel gating structure discussed in Section 5 is used. It is the most simple and direct of the three transfer schemes considered.

A large-geometry buried-channel to surface-channel test structure was included to allow testing of the buried-channel to surface-channel transfer concept using Scheme 1. (Conceivably, this could have been done using the main array, but it would have been difficult because of the smaller yield on the main array and the more difficult testing associated with it.) This device is made of adjacent 16-bit buried-channel and surface-channel registers with appropriate transfer gates in between. The cell dimensions were somewhat larger than those for cells used in other test structures: this was done to minimize the photolithography requirements. A detailed photograph of this test structure is shown in Figure 9.

The 3 x 30 SPS array is identical to the 64 x 64 array in construction except that 61 parallel columns and 34 rows have been removed and a different buried-channel to surface-channel transfer scheme has been used. This was a backup to Scheme 1.

The 3 x 40 SPS array was designed to serve the same purpose as test circuit 3 in that it uses a third scheme for achieving the buried-channel to surface-channel charge transfer.

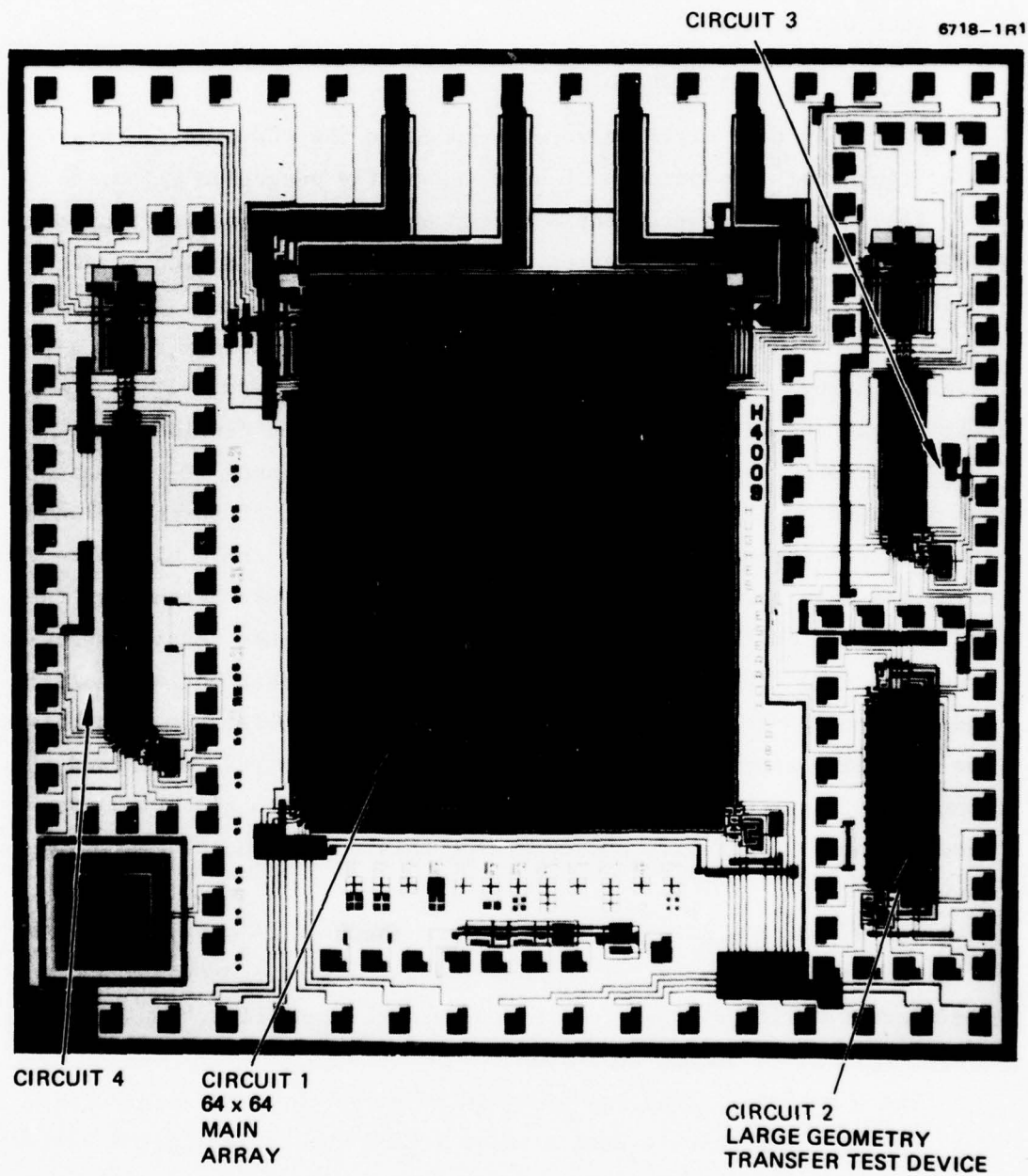


Figure 8. Photograph of CCD chip indicating the four major circuits on the chip.

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Figure 9.

Large geometry buried to surface channel transfer circuit showing A, 16 bit buried channel register; B, 16 bit surface channel register; and C, 3 transfer gates (i.e., blocking gate, transfer gate, and surface gate 1).

SECTION 2

PROGRAM SUMMARY

A. GOALS

The overall objective of this program was the continued development of the CCD LCLV. The task was to evaluate the existing CCD chips, to fabricate light valves, and to make recommendations for the design and chip-processing modifications for the second option of this program. The existing CCD chips were fabricated according to the original design. Therefore, the chip fabrication under the second option will be the first iteration of the CCD LCLV design for this complicated device. This objective was divided into two areas of investigation. The first involved the CCD array on the front side of the wafer, while the second involved primarily the backside MOS readout structure.

At the start of this program, all of the essential features of the CCD array had already been demonstrated on a previous DARPA contract (DAAG53-76-C-0066). That contract had concluded that all of the unique design features incorporated into the CCD input registers and arrays were functional and hence that no major redesign of any structure was required. At that time, very little quantitative information was available on the level of performance for the various features and structures on the CCD input device. Such items as the BCCD input register transfer efficiency, the input signal linearity, and the efficiency of transfer from the buried to surface channel structures required a more quantitative assessment to understand fully the performance of this device.

Additionally, all of the performance information reported on the previous DARPA contract had been obtained from a few samples fabricated on Lot No. 3. This group of 20 wafers contained only four wafers with any working devices, and of those devices only a few were functional. Thus, the statistical base for the reported measurements was limited. On the present program, our aim was to use wafers and devices from Lot No. 4, the last completed run on the previous contract. On wafers tested from that run, we had observed that as many as 60% of the chips on a given wafer were completely functional and that all of the wafers

that had been tested contained at least five operational CCD devices. Thus, it was our intention on the present program to use devices exclusively from this run to obtain a sounder statistical basis for the measurements of CCD performance parameters.

A second major goal in the present program was to demonstrate a completely operational CCD LCLV. At the end of the previous contract, we had demonstrated minority-carrier charge transfer from the CCD side of the chip to the readout side MOS structure by utilizing the entire CCD parallel array as a single storage element. In this mode of operation, charge is actively and directly loaded into the storage element by process of the input gating structure without the intervening process of peristaltic transfer through individual CCD cells. With this type of signal introduction, we were able to demonstrate that sufficient charge can be transferred to activate the liquid crystal and that this basic scheme for electrical-to-optical conversion is sound. We were not able to load data into individual cells of the CCD parallel array and then transfer that spatially resolved data field to the liquid crystal. Since we were not able to see any optical effect from the transfer of signal from the parallel array, we were not able to assess the actual or potential spatial resolution limitation of the MOS readout structure. Thus, the primary objective of the present program was to demonstrate that signal charge could be loaded into the parallel array, subsequently transferred to the liquid crystal, and thereby produce a spatially resolved optical image from that original data pattern.

B. ACHIEVEMENTS AND CURRENT STATUS OF THE CCD LIGHT VALVE

This relatively short program led to several significant achievements and milestones in the continuing development of the CCD LCLV. We have:

- Demonstrated a fully operational CCD LCLV with a spatially resolved output corresponding to the input data pattern (50:1 contrast ratio, 12 resolution lines across the device).

- Developed an improved dicing method which has increased fill time from 5 msec to 500 msec.
- Developed improved packaging, which has increased the packaging yield from 30% to 80%.
- Measured the buried to surface channel transfer efficiency with values in excess of 95%.
- Measured the buried channel charge transfer efficiency on the large geometry transfer test device (LGTTD).
- Assessed several alternative input-loading schemes for improved analog signal linearity on the SCCD serial input register.
- Determined the effect on serial transfer efficiency resulting from the Si/SiO₂ interface states.

The success of the buried-channel to surface-channel charge-transfer scheme was one of the first milestones achieved. Recent measurements on this structure indicate that signal charge can be transferred from the buried to the surface channel device with an efficiency of greater than 95%. Further electrical characterization of the CCD wafers from the first three lots confirmed the success of the other novel ideas. The high quality of the buried- and surface-channel CCDs demonstrated that the wafer thinning done mid-processing did not deteriorate these circuits. The high quality of the CCDs is illustrated by the attainment of a charge transfer efficiency in the surface channel of 0.9998. The electrical testing has also shown that the semiconductor processing used to produce the CCD circuits did not significantly degrade the high resistivity and minority carrier lifetime of the bulk silicon.

In an analogous and concurrent project on the photoactivated silicon LCLV, a project in which the same readout mechanism is used as in the CCD/LCLV, we have been able to demonstrate that the maximum achievable spatial resolution is determined primarily by the cell size of the micro-grid structure. In addition, the focusing effect associated with this structure has been demonstrated on the photoactivated silicon light valve.

On the photoactivated Si LCLV, we have also changed the dielectric mirror from the ZnS/NaAlF_4 pair to an evaporated poly Si/SiO_2 structure. This significantly reduced the chemical degradation associated with the liquid crystal and allowed post-deposition annealing procedures to be used for removing the wafer damage incurred during the cermet light-blocking layer (LBL) and dielectric mirror (DM) depositions. With these anneals, we have been able to demonstrate an 80% reduction in the thermally generated dark current on this device, which translates directly to a projected factor of five increase in input sensitivity on the CCD LCLV program.

Finally, we have conclusively demonstrated an operational CCD/LCLV. With this device, we were able to show the direct conversion of a serial electrical input signal to a parallel optical output image. Data was loaded into the 64×64 element parallel array using the surface channel serial input register. The best spatial resolution observed with this particular device was five CCD lines, which were transferred into one output image line. The output contrast ratio for this limiting data pattern was found to be approximately 4:1. This parameter increased to above 50:1 when full frames of signal were transferred to the liquid crystal. In the latter operating mode, the linearity of the electrical-to-optical conversion was good over a fairly wide portion of the output dynamic range.

Although we have demonstrated all of the essential operating features of the CCD LCLV, there still remains the overall task of optimizing the readout structure to achieve full resolution and sensitivity and of amalgamating the diverse features of this device into a fully operational CCD LCLV.

C. RECOMMENDATIONS

During this program, it became evident that the major problems affecting the overall performance of the CCD LCLV were the limitations existent with the MOS readout structure and the associated process of efficiently transferring signal charge from the CCD array to the liquid crystal. All of the essential features of the CCD input and storage

devices have been successfully demonstrated. Quantitative information on the performance parameters for both the BCCD and the SCCD serial input registers, the SC parallel array, and the BC/SC transfer device have been obtained. In all cases these parameters were found to be more than adequate to meet the performance specifications for the present CCD LCLV.

The only major parameter associated with the CCD structure not yet evaluated is the upper frequency limit of the BCCD serial input register. All of the testing to date on this device has been at relatively low frequencies, where instrumentation such as clock drivers and signal charge amplifiers are readily available. Equipment limitations are the major reason why we have not yet determined the frequency limitations for this structure. We do not now have the necessary drivers and output amplifiers to adequately test this device at frequencies at or near the design goal of 100 MHz. To accomplish this specific task, custom test instrumentation would have to be designed, built, and tested for this purpose since such equipment is not now commercially available. Since we felt that this measurement would have seriously diverted our efforts from the overall goal of demonstrating a functional CCD LCLV, this task was not undertaken. There is ample evidence¹⁻⁶ in the literature to confirm our position that the goal of 100-MHz BCCD operation is both realistic and achievable with present day technology. Therefore, our present recommendation would be to postpone addressing this problem until the other major structural and device problem areas have been developed to the point where the BCCD frequency limitations are a major limitation to the performance and system utility of the CCD LCLV.

To fulfill the overall performance goals for this device, we suggest that the next program concentrate on the problems and limitations associated with the MOS readout structure and its adjacent thin-film cermet LBL and DM. Since the available signal charge is limited by the size of parallel array CCD cells, the efficiency of charge transfer from the storage array to the liquid crystal layer is an important question. In addition, the spatial resolution of the signal charge, defined initially by the geometrical dimension of the parallel array, must be maintained during and after the signal-transfer process. The

latter issue becomes even more important when the next generation of CCD LCLV devices (i.e., 256 x 256 and 1000 x 1000 pixels) are considered. To address both problem areas, the following tasks are currently under investigation and/or recommended for next developmental programs, which will be the first iteration of the original design.

- Substrate degradation due to the radiation damage in Si generated during the deposition of and stresses associated with the thin film LB and DM layers. This effect will be eliminated by using the novel Si/SiO₂ mirror and by implementing an appropriate annealing process. The effectiveness of this solution has been demonstrated on the photoactivated light valve.
- Edge breakdown, which limits the maximum applied readout voltage to values insufficient for full depletion through to the epitaxial layer. This problem will be eliminated by implementing the np diode guard ring which was originally designed for the CCD LCLV and was successfully tested on the photoactivated LCLV.
- Lifetime and substrate resistivity degradation associated with the many high-performance semiconductor processing steps required to fabricate the CCD structure. To achieve the improvement, all processing steps will be carried out at temperatures below 1000°C and HCl oxide will be implemented.
- Epitaxial layer resistivity and thickness should be optimized for maximum spatial resolution and signal transfer efficiency.
- Alternative readout structures such as the MOS/PN junction approach, which has recently been successfully demonstrated on the concurrent photoactivated silicon light valve program.

The following sections describe in more detail the present program and make recommendations for the next phase of the program.

SECTION 3

ELECTRICAL CHARACTERIZATION OF CCD WAFERS

A. BURIED-CHANNEL AND BURIED-TO-SURFACE-CHANNEL TRANSFER EFFICIENCY MEASUREMENT

The buried-to-surface-channel transfer and the BCCD serial charge-transfer process were evaluated using the large geometry transfer test device (LGTTD), shown as Circuit 2 in Figure 8. An expanded view of this test structure is shown in Figure 9. The LGTTD and the actual transfer structure used on the main array differ in several significant ways:

- The LGTTD input and output registers are only 16 bits long versus 64 bits on the main array.
- The LGTTD transfer device has only one surface gate versus two on the main array.
- Each gate on the LGTTD has an area twice that of the corresponding gate on the main array.

These differences simplify the evaluation of the BCCD serial transfer and the buried-to-surface-channel transfer (BC/SCT) processes without camouflaging the performance of the analogous BC/SC transfer structures on the main array. The only compromising feature of the LGTTD concerns the measurement of the charge-transfer efficiency of the BCCD serial input register. Since the buried channel gates are twice as long, the efficiency of the fringing fields in transferring charge is expected to be somewhat lower. This implies that the charge-transfer efficiency and the upper frequency limit for this LGTTD BCCD will probably both be lower than the corresponding parameters on the main array BCCD. Hence the measurements on the LGTTD in the worst case can only yield an overly conservative evaluation of the LGTTD BCCD performance.

There are three potentially useful schemes for transferring charge from the buried to the surface channel structures. Each scheme has been included on this chip as peripheral test circuits, Circuits 2, 3, and 4 on Figure 8. To understand the difficulty, consider the

straightforward approach (Figure 10). In this method, a transfer gate located directly over the surface metallurgical p-n junction is used to control the flow of signal charge between the buried and surface channels. A schematic of this transfer structure is shown in Figure 10. The structure, from left to right, consists of a buried-channel gate (BG), a transfer gate (TG), and a surface collecting gate (SG). (The direction of charge propagation in the buried channel is perpendicular to the plane of the paper.) The operation of this structure is illustrated in Figure 11, which shows the electron potential, ψ , versus distance into the substrate, X , at various points along the device for the gate voltage relationships indicated. If any charge were stored under the buried-channel electrode, it would flow to the lower potential minimum under the transfer gate. A comparison of $\psi_c(x)$ with $\psi_b(x)$ shows that $\psi_c(x) > \psi_b(x)$, regardless of the transfer gate voltage V_{TG} ; therefore, there is a potential barrier preventing electron flow to the surface gate electrode. The solution to this problem is to increase the buried channel gate width L_B sufficiently so that L_B is much greater than L_G , the width of the transfer gate over the buried channel. Transfer can then occur because there will be sufficient charge available to raise the potential $\psi_b(0)$ to $\psi_c(0)$, at which point electrons will spill over into the surface collecting electrode. A certain amount of charge will remain in the buried channel under the transfer gate (i.e., all the charge required to raise $\psi_b(0)$ to $\psi_c(0)$). However, since $L_B \gg L_G$, the remaining charge under the transfer gate can be small compared with the total charge transferred (assuming that the buried channel is operated at near full capacity). Once this charge has been transferred to the surface electrode, the charge can then be clocked conventionally onto a surface channel.

From the previous discussion, it is evident that there will be some degradation in transfer efficiency from the buried channel to the surface channel, as a result of charges trapped under the transfer gate. A "fat zero" equal to the trapped charge could be introduced, but the

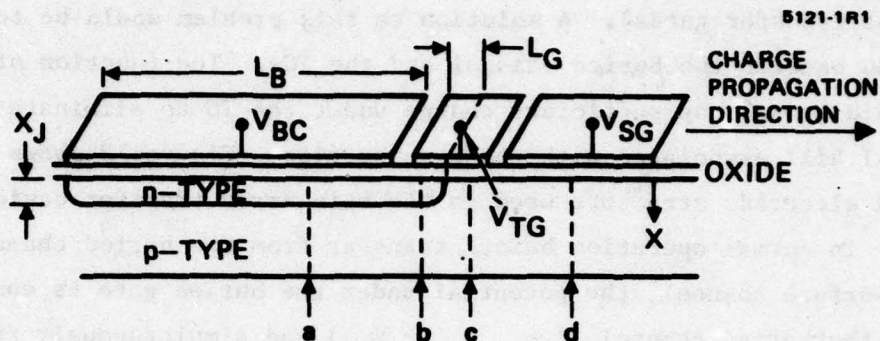


Figure 10. Possible gate structure for the transition from the buried channel to the surface channel.

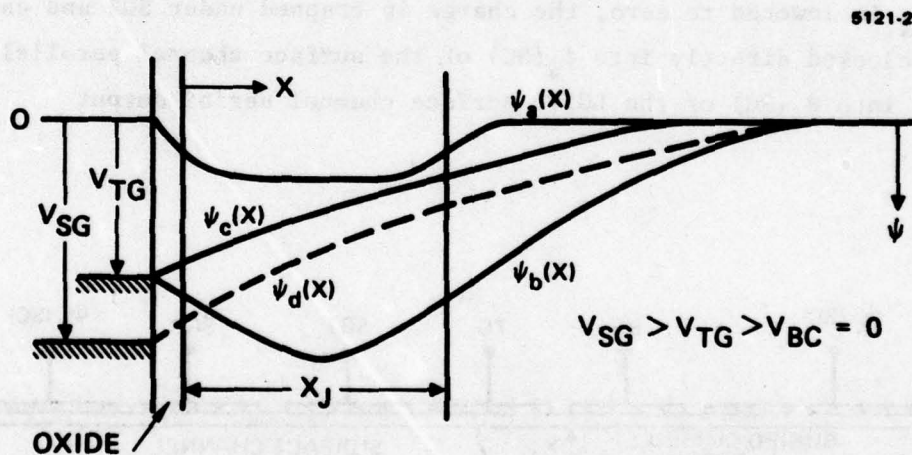


Figure 11. Potential ψ versus distance x into substrate. $\psi_a(x)$ is drawn assuming some electron charge is contained. $\psi_b(x)$ is drawn assuming no electron charge is contained.

improved transfer efficiency would probably be offset by increased fixed pattern noise (different quantities of electrons would be trapped under different transfer gates). A solution to this problem would be to introduce a BG between the buried channel and the TGs. The function of this gate would be to trap sufficient charge under the TG to eliminate the potential hill associated with the p-n junction. Figure 12 shows the modified electrode structure used on the main array transfer device (MATD). In normal operation before transfer from the buried channel to the surface channel, the potential under the buried gate is enough to isolate the buried channel (i.e., $\psi_{BG} > \psi_{BC}$) and simultaneously prevent charge trapped under the TG from flowing back onto the buried channel. Transfer from the buried channel to the surface channel is achieved by increasing ψ_{BC} (decreasing V_{BC}) until $\psi_{BC} > \psi_{BG}$. Charge will then spill over the region under the blocking and transfer gates into the region under the second surface gate because ψ is lowest there. When V_{SG1} is lowered to zero, the charge is trapped under SG2 and can then be clocked directly into $\phi_4(SC)$ of the surface channel parallel array or into $\phi_4(SC)$ of the LGTTD surface channel serial output register.

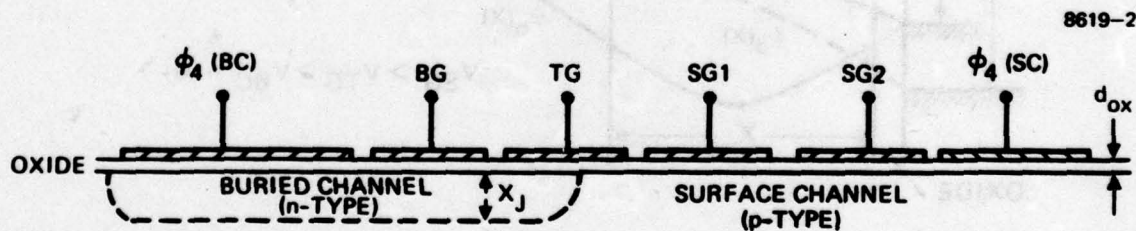


Figure 12. Schematic of the improved BC/SC main array transfer structure which utilizes a blocking gate (BG) to eliminate signal charge trapping under the transfer gate. Surface gate (SG2) is not present on the LGTTD.

The experimental arrangement used for both measuring the BC/SC transfer efficiency, η_T , and the BCCD charge transfer efficiency, η_{BCCD} , is shown in Figure 13. The various clock and gating waveforms used for the η_T measurement are shown in Figure 14. All of the timing required to realize these waveforms is provided by the multichannel programmable word generator (Interface Technology RSM-432); the variable pulse amplitudes for each of the signal lines are generated by the array of clock drivers (Pulse Instruments PI451). To eliminate the need to calibrate the conversion gain factor of the SCCD output amplifier, which basically functions as a charge-sensitive integrating amplifier, the output signal charge is measured directly by using the V_{DD} diffusion as an output diode. This alteration requires that the reset gate be continuously turned on to provide an Ohmic connection between the floating and V_{DD} diffusions. For the BCCD register, the charge is collected directly using the output diode incorporated on that structure.

The measurement of η_T is performed in three parts. First, a data block of 16 bits is loaded into the BCCD with the sequence of clock waveforms AAA...A shown in Figure 14. Then the gate controlling the input data is turned off, and the stored data pattern can then be clocked out of the BCCD by the sequence of 16 clock cycles CCC...C. This double sequence of events AA...ACC...C is referred to as Mode 1. Alternatively, after the loading sequence AA...A, the 16 bits of data in the BCCD can be transferred in parallel to the SCCD register during the time interval B. The transferred data is now clocked out of the SCCD using the 16 clock cycles CC...C. This triple sequence for the BC/SC transfer AA...ABCC...C is referred to as Mode 2. During the transfer sequence B, the buried, transfer, surface, and the ϕ_4 (SCCD) gates are all simultaneously activated with voltages satisfying the relationship $V_{BG} \leq V_{TG} \leq V_{SG} < V\phi_4$ (SCCD). Subsequently, the gate voltage of ϕ_4 (BCCD), under which the signal charge in the BCCD is stored, is then lowered to effectively raise the BCCD channel potential so that the stored charge can now flow freely to gate ϕ_4 (SCCD). The buried, transfer, and surface gates are then switched off sequentially, which forces any residual signal charge into ϕ_4 (SCCD).

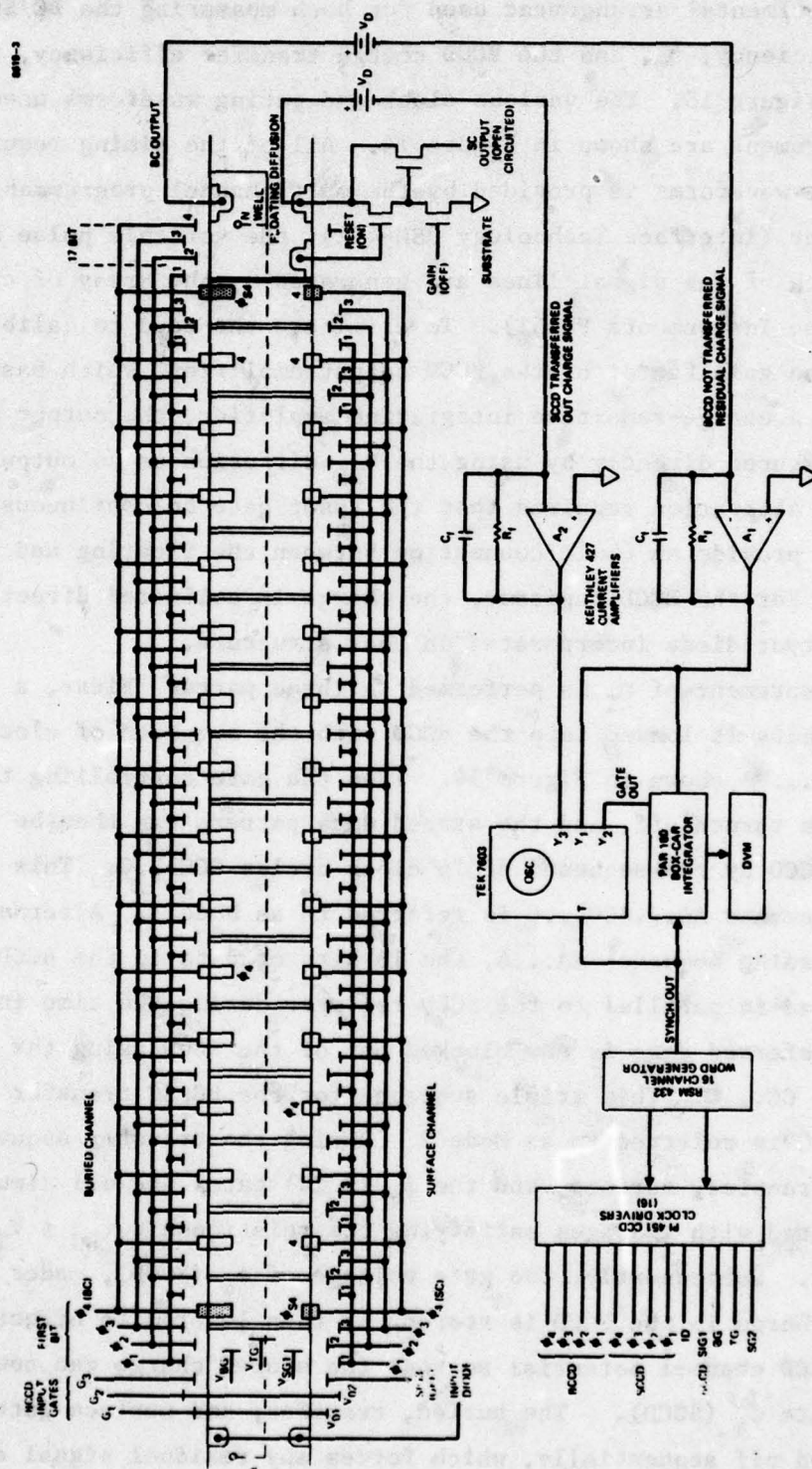


Figure 13. Large geometry transfer test device (LGTTD) schematic and experimental arrangement for the measurement of the BC/SC transfer efficiency (η_T) and the BCCD serial charge transfer efficiency (η_{BCCD}).

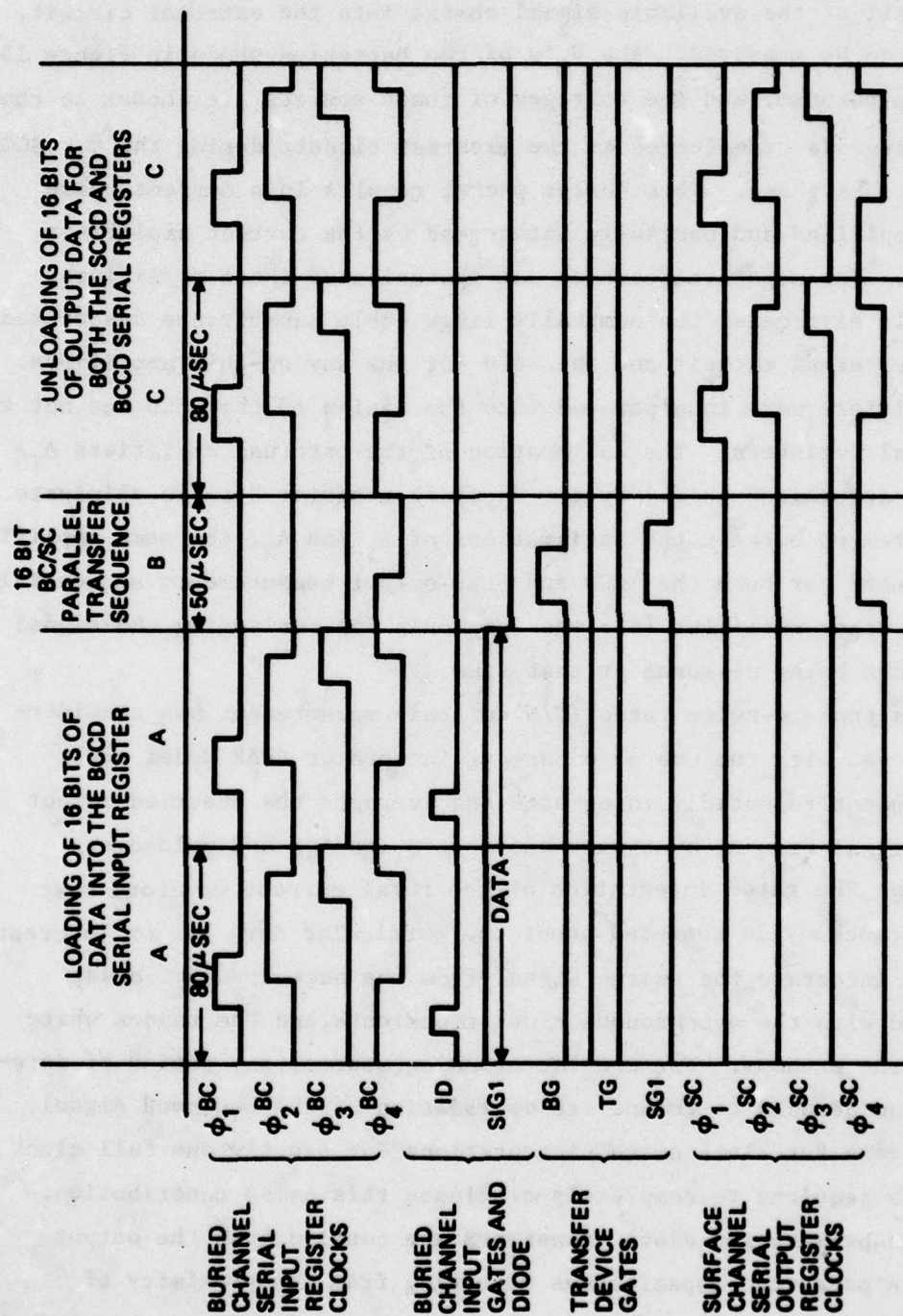


Figure 14. Clock and associated LGTTD gate waveforms used in the BC/SC transfer efficiency experimental arrangement of Figure 13.

In the measurement of signal charge emanating from either the BCCD or the SCCD registers, the output diodes must be sufficiently back biased to force all of the available signal charge into the external circuit, where it can be measured. The V_D 's of the batteries shown in Figure 13 serve this purpose, and the voltages of these sources are chosen so that signal charge is transferred to the external circuit during the ϕ_4 (SCCD or BCCD) clock phase. This charge packet results in a current pulse that is amplified and partially integrated by the current amplifiers A_1 and A_2 . The negative feedback configuration of these amplifiers effectively eliminates the nominally large cable capacitance associated with the external circuit and the need for the any on-chip amplifiers. Such amplifiers were incorporated into the design of the SCCD but not the BCCD serial registers. The calibration of the external amplifiers A_1 and A_2 is determined solely by the feedback resistor R_f . To eliminate any differences between the calibrations of A_1 and A_2 , the same amplifier (A_2) was used for both the BCCD and SCCD output measurements sequentially while the other amplifier (A_1) was used only for monitoring the signal that was not being measured at that time.

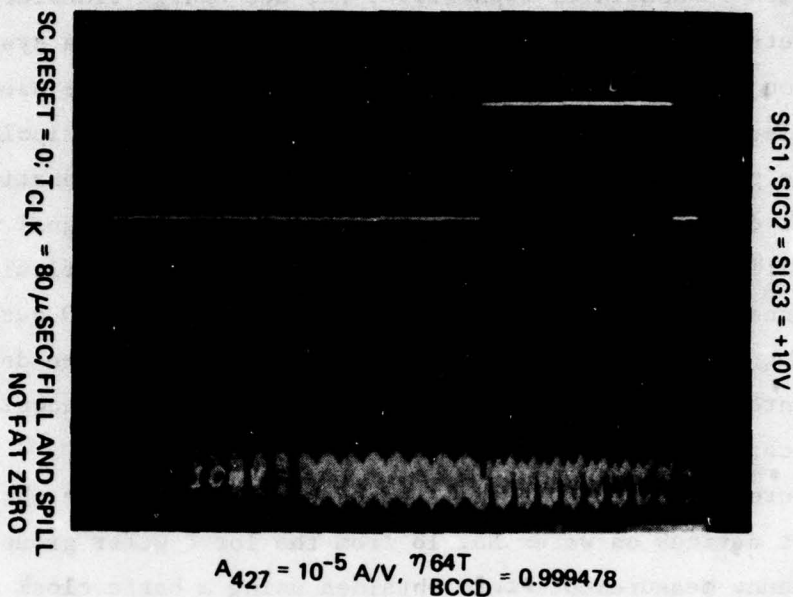
The signal-to-noise ratio (S/N) of this measurement was considerably improved with the use of a box-car integrator (PAR Model 160). This instrument repeatedly integrates and averages the observed output current signal from A_1 over many successive loading and unloading sequences. The gated integration of the total current waveform over one full clock cycle centered about the particular data bit of interest serves to integrate the charge signal from the background of noise associated with the synchronous clock transients and the random white noise of the preamps. For the latter noise source, any period of integration can be used to reduce its degradation of the observed signal. Alternatively for clock noise, integrations for exactly one full clock period are required to completely eliminate this noise contribution. This is so because the clock transients are coupled into the output signal via parasitic capacitances resulting from the proximity of clock and signal lines on the chip itself and the testing probe card used to make electrical contact to the device. Thus, since this noise

contribution is basically capacitive, the net charge transferred over one complete cycle must of necessity equal zero. Hence a synchronous integration over one or more complete clock cycles can be used to cancel this bipolar clock noise current while integrating the unipolar signal current to provide a measure of the set signal charge emanating from the CCD output device. When viewing the total noise plus signal waveform from amplifier A_1 on an oscilloscope directly, it is difficult to detect the presence of any charge signal, especially on the SCCD output, which is camouflaged by clock noise. Alternatively, by using the described sampled integration scheme of Figure 13, we are able to acquire the measured charge with a S/N in excess of 60 dB.

Measurements of BCCD serial transfer efficiency were obtained from LGTTD test devices on wafer No. 18 from the lot 4 wafer group. Only low-frequency measurements were obtained using a basic clock repetition rate of 12.5 kHz. This limitation was imposed by the use of the Keithley 427 current amplifiers (A_1 and A_2 in Figure 13), which are restricted to frequencies of less than 15 kHz on the sensitivity range needed in these measurements. The serial transfer efficiency was calculated from the expression

$$\eta_T = (Q_1/Q_2)^{1/T} \quad (1)$$

where Q_1 and Q_2 are the charge amplitudes of the first and second bits of the output signal data pattern, and T is the total number of transfers associated with the particular shift register under test. On several devices from this wafer, we measured a serial charge transfer efficiency, η_T (BCCD), equal to 0.99946 ± 0.000027 . The output data pattern of the BCCD register is shown in Figure 15, where the amplifier time constant was chosen to minimize clock noise. We also found that the observed value of η_T (BCCD) was not strongly dependent on the individual clock voltage amplitudes. That observation supports our original belief that the fringing field transfer mechanism does not play a significant role in the operation of the LGTTD BCCD serial input register. This then allows us to postulate that the shorter channel CCD cells used



Top Trace:

Input data signal applied to SIR Gate 1 which corresponds to the loading of 8 full buckets followed by a sequence of 24 empty buckets.

Bottom Trace:

Output signal current waveform from amplifier A_1 with sensitivity 1×10^{-7} A/cm. The feedback time constant of A_1 and the BCCD four-phase clock amplitudes and frequency are specifically chosen here to provide a high degree of clock noise rejection. Using Eq. 1 we can calculate an $\eta_T(\text{BCC}) = 0.99948$ from these data.

Figure 15. LGTTD BCCD serial input register operation. ($f_{\text{CLK}} = 12.5$ kHz, fill and spill loading without fat zero.)

on the main array BCCD should have higher η_T (BCCD) because of the expected greater relative importance of the fringing field transfer mechanism in these structures. In fact, we have measured on the main array transfer efficiencies of 0.99994 in the BCCD.

We also observed that no significant improvement occurred in the measured value of η_T (BCCD) with the use of the so-called "fat zero" input signal loading technique. This technique is often used to improve η_T on SCCDs where it provides a background source of residual free carriers from which the omnipresent interface states can be filled. Hence the surface states are continually occupied, eliminating the need to periodically refill them when the analog data signal is transferred from one cell to the next. In addition to higher SCCD transfer efficiencies, the use of the fat zero also results in higher frequency operation. The penalty incurred by incorporating the fat zero is a reduction in the available dynamic range. That we found no improvement in η_T (BCCD) with the incorporation of the fat zero suggests that the BCCD channel is located sufficiently deep in the epilayer so that surface states do not contribute to the observed transfer efficiency. If the BCCD channel were located near the Si/SiO₂ interface, then, for large signal levels, some of the charge would be stored at the surface and the measured large-signal η_T would be lower than the corresponding small signal η_T . Thus, the observed independence of η_T with respect to the fat zero allows us to conclude that the junction depths for the devices tested here are large enough to yield complete BCCD operation for full buckets of data. Since no conclusion as to whether these junctions are deep enough to achieve the 100-MHz upper frequency limit can be obtained from this data, the question remains open.

The buried-channel to surface-channel transfer efficiency measurements were conducted as they had been with the LGTTD structures. The signal charge contained in a given cell of the BCCD before transfer is first measured by serially shifting the charge out through the BCCD output diode using the mode/clocking scheme (described above). Then the BCCD register is reloaded with signal charge, and the SPS transfer is accomplished using the Mode 2 clocking sequence. The transferred

signal charge is again measured by serially shifting out each bit of data via the modified SCCD output diode. For the experimental results reported here, both the BCCD and SCCD registers were clocked at 12.5 kHz, while total SPS transfer time was arbitrarily chosen to be 50 μ sec. In these measurements, we observed transfer efficiencies of 90% to 105%; an efficiency greater than 100% implies that more charge came out of the SCCD register than was thought to be in the corresponding bit of the BCCD register. It should be emphasized that the charge content of any given BCCD cell was implicitly determined by not performing the SPS transfer and instead measuring the output charge for each bit of the BCCD register. The measured value of ϕ_T (SPS) is dependent on the bit position in the SCCD register. Hence, for SCCD bit number 1, which must be transferred through 16 cells before its charge content can be determined, we observed an ϕ_T (SPS) of 90%. The highest transfer efficiency, 105%, was observed for bits near the end of the SCCD register; those bits do not have to be transferred as many times before their signal charge is measured. This bit-position-dependent ϕ_T (SPS) characteristic can be completely accounted for by the relatively poor transfer efficiency (0.997) of the SCCD register associated with the particular type of clocking used in these experiments. (Section 2.B discusses this point further.) The transfer characteristic for bit number 16 relating both the BCCD and the SCCD output charge magnitudes to the input signal voltage (SIG 2,3) is shown in Figure 15(b). Here both Q_{BCCD} and Q_{SCCD} scale approximately linearly for input signals within the range from 6 V to 10 V. Above 10 V, the output charge magnitudes remain constant for additional increases of input signal; below 6 V, no charge can be loaded into either the BCCD or the SCCD registers. This transfer characteristic is quite similar to the behavior described in Section 3.B, where several alternative SCCD loading methods are investigated on the main array SCCD serial input register.

The observed values of buried-to-surface transfer efficiency in excess of 100% are undoubtedly an effect of the indirect method used to measure the charge in the BCCD buckets before the parallel transfer. It is possible that a small percentage of the actual charge is loaded into

the transfer structure during the serial in/serial out operational mode. If this were to occur, it would appear that a smaller packet of signal charge resides in each BCCD bucket before transfer and hence that the transfer efficiency was greater than 100%. The postulated leakage of BCCD charge could possibly occur if the blocking gate were not totally effective in providing the required potential barrier during the BCCD loading process. With this situation, we would expect that the net charge leakage would be more severe for full buckets than for relatively empty levels of input signal. From the data shown in Figure 16, it appears that this is not the case and that the observed net charge difference $\Delta Q (= Q_{\text{SCCD}} - Q_{\text{BCCD}})$ is much larger for smaller input signal amplitudes than for the apparent full buckets associated with the saturated region of this curve. It is also possible that the buried pn junction leakage current is responsible for the loss of BCCD signal charge, but it is not at all clear how this mechanism could result in the eventual transfer of this lost charge to the SCCD. Even with this unresolved question as to the exact numerical value of η_T (SPS), we can safely assume that the main transfer structure functions as expected from its design considerations and that the true SPS transfer efficiencies are at least 95%.

B. SURFACE CHANNEL CCD SERIAL INPUT REGISTER

This section describes the results from two series of measurements on the main array SCCD serial input register (MA SCSIR). These investigations concerned the role of interface states in determining the serial charge transfer efficiency for the SCCD devices on this chip. In addition, the investigations sought to determine linearity relationships between the input and output data signals for several alternative SIR loading schemes. These relationships are important in any analog signal-processing application where the degradation of the output data fidelity resulting from system nonlinearities can ultimately restrict the use of this device in any practical application. We chose to direct our attention in this series of experiments to the MA SCSIR structure since that

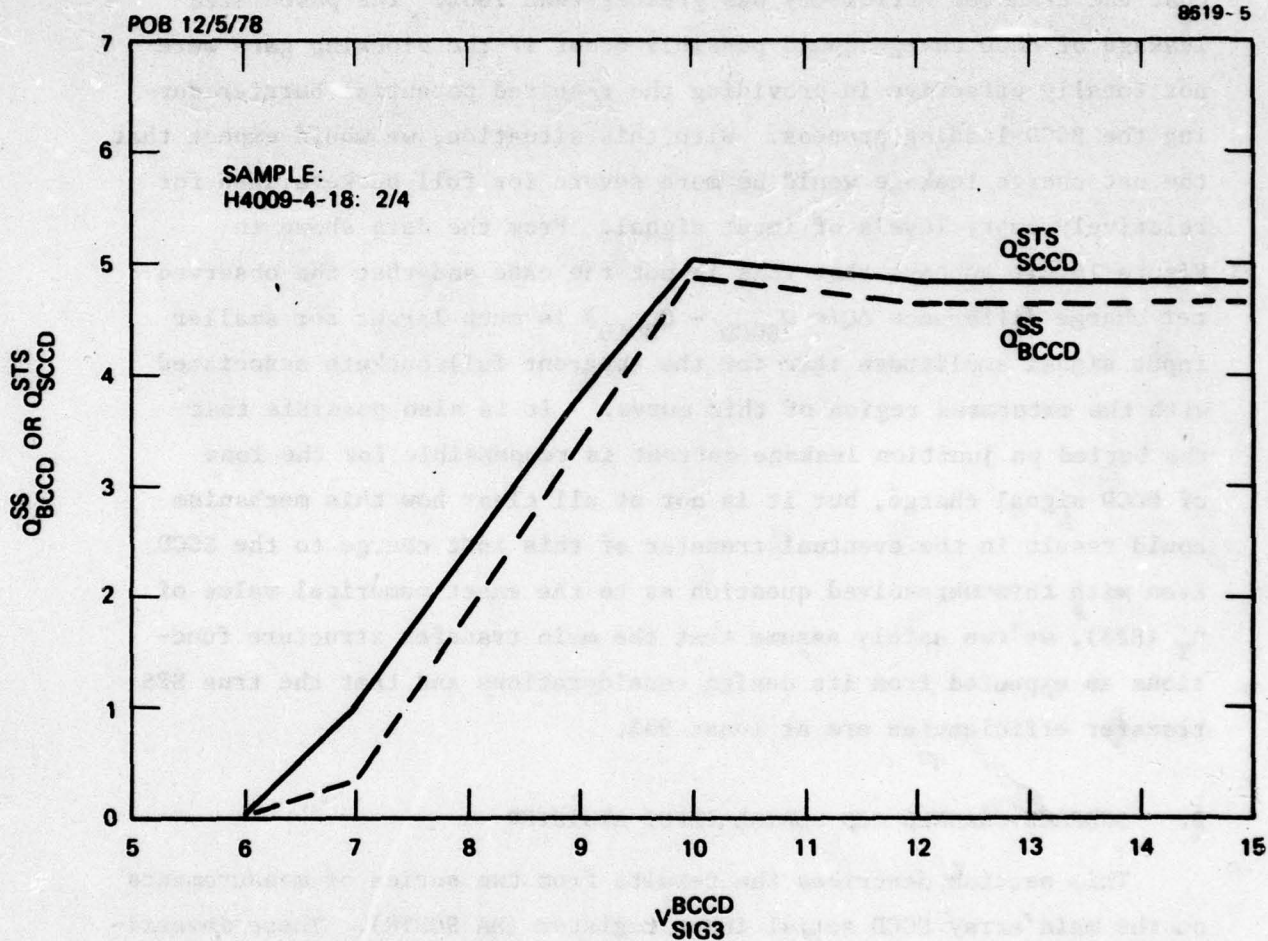


Figure 16. Transfer characteristic relating the output change amplitudes from the BCCD and the SCCD registers to the analog input signal voltage on gate SIG3. f_{clk} (BCCD and SCCD) = 12.5 kHz. $T_{transfer}$ = 50 μ sec.

device has been used exclusively for loading data into the CCD LCLV parallel array. This option allows us to test the complete CCD LCLV without the complications introduced by the BCCD and the BC/SC transfer operation. Therefore, the characteristics of the MA SCSIR are important for interpreting the performance of the CCD LCLV.

Both the transfer efficiency η_T (SCCD) and linearity of the SCCD were measured using the experimental arrangement shown in Figure 17. The major difference between this apparatus and that shown in Figure 13 for measurements on the LGTTD is the use of the on-chip SCCD output amplifiers. This device is essentially a charge-to-voltage converter and amplifier that allows us to transform the small output charge signal to a voltage with a source impedance that is low enough to drive coaxial cables and to minimize the effects of capacitive coupling from adjacent clock lines. In addition, a ramp generator is included to continuously vary the pulse amplitudes applied to the serial input gates (SIGs) for the linearity measurements. The clock and timing waveforms for these experiments are described in Figure 18. The SIG loading signals are specially shown for the SCCD transfer efficiency measurements, where the input loading scheme, which had been shown to provide the best analog signal linearity, was used exclusively.

We made serial transfer efficiency measurements to determine the relative importance of surface states on the value of η_T (SCCD). To accomplish this task, measurements of η_T (SCCD) were obtained both with and without the use of a fat zero. This technique (discussed in Section 3.A) can be used to neutralize the deleterious effects of such interface states on both η_T and on the upper frequency limit for this device. The clock waveform used in most of the experiments on this program were such that the individual MOS gates were switched from a condition of surface accumulation to depletion and vice versa. In this operating mode, holes are attracted to the Si/SiO₂ interface during the accumulation phase of each cycle; at the interface they recombine with minority carriers trapped in the surface states. Hence, the interface traps are discharged on each half cycle and therefore are ready to acquire charge from the signal in the next bucket. This is the major mechanism

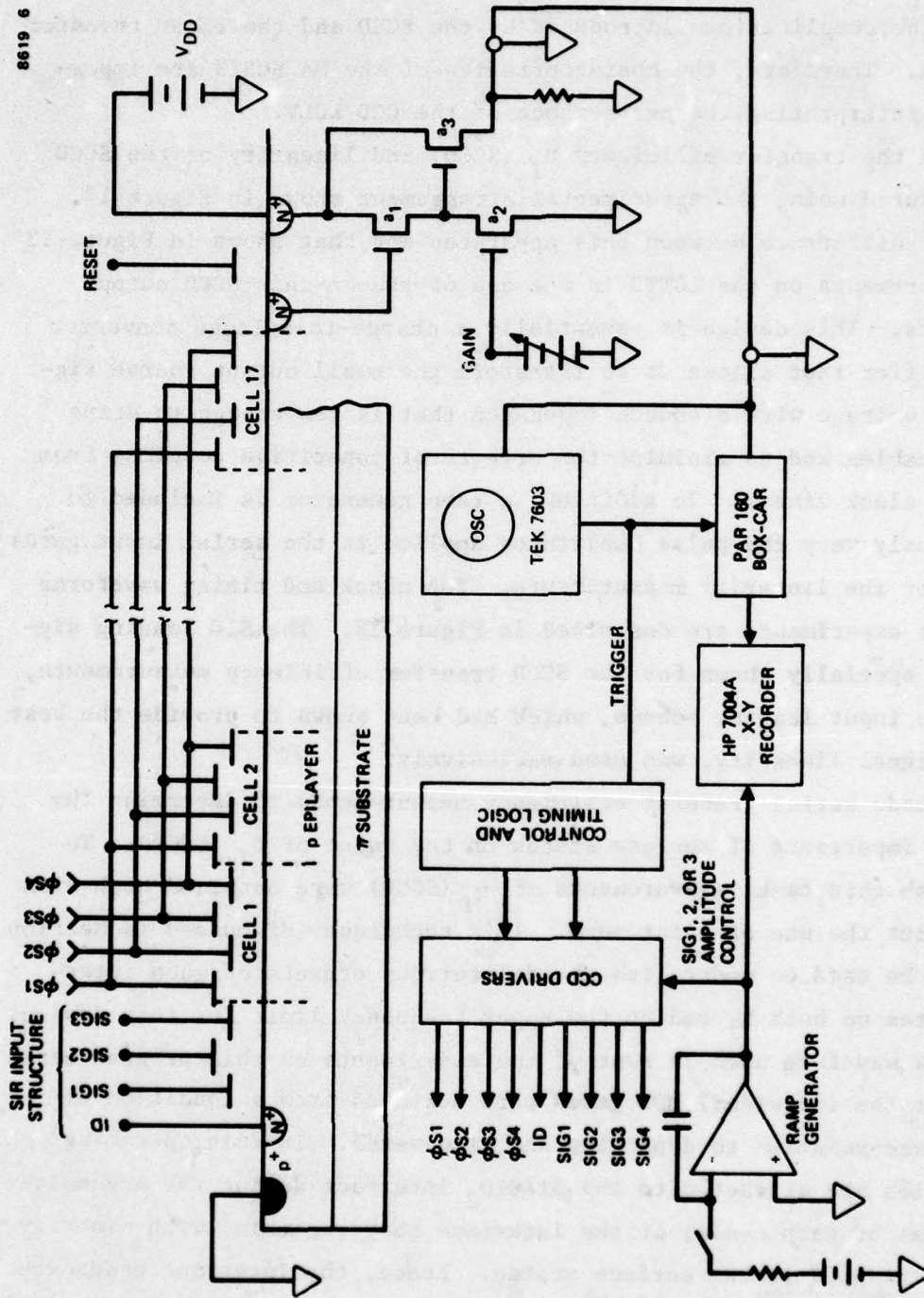


Figure 17. Serial SCCD input register testing: experimental arrangement for the transfer efficiency and linearity measurements on the SCCD serial input register.

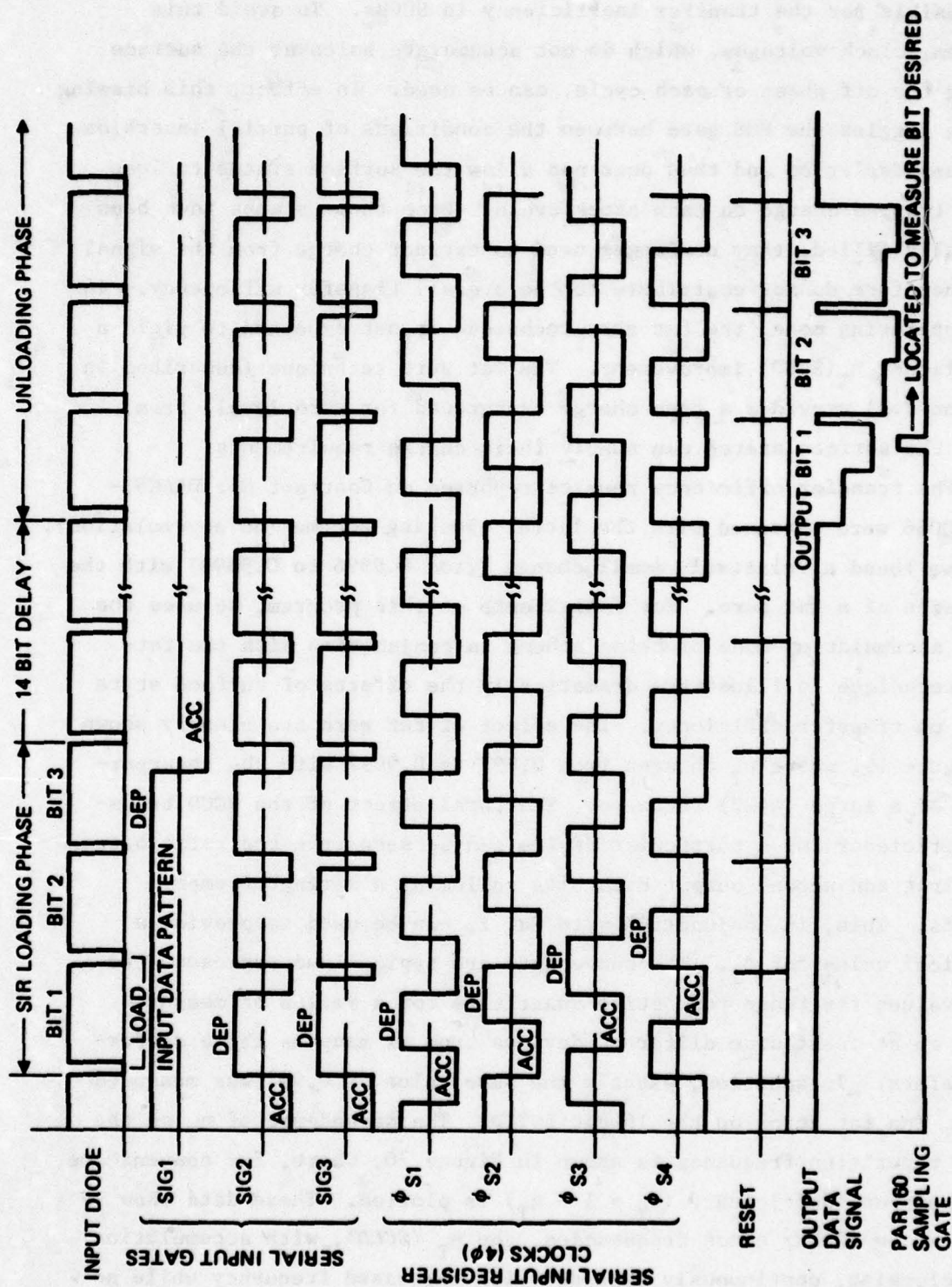
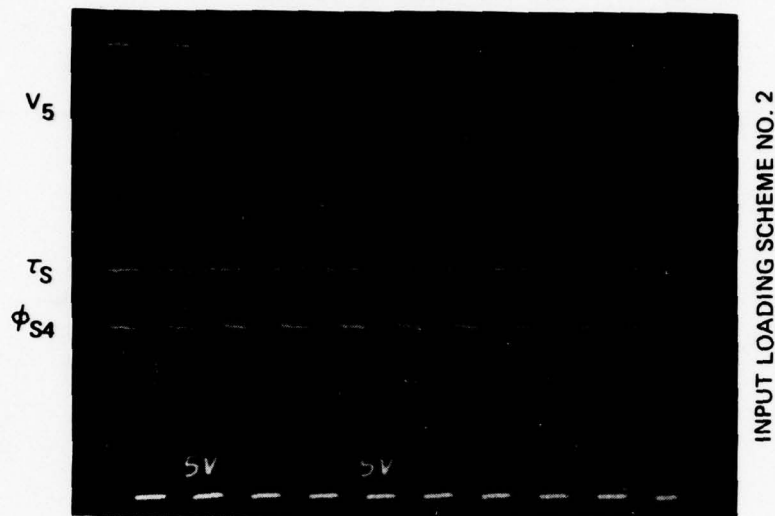
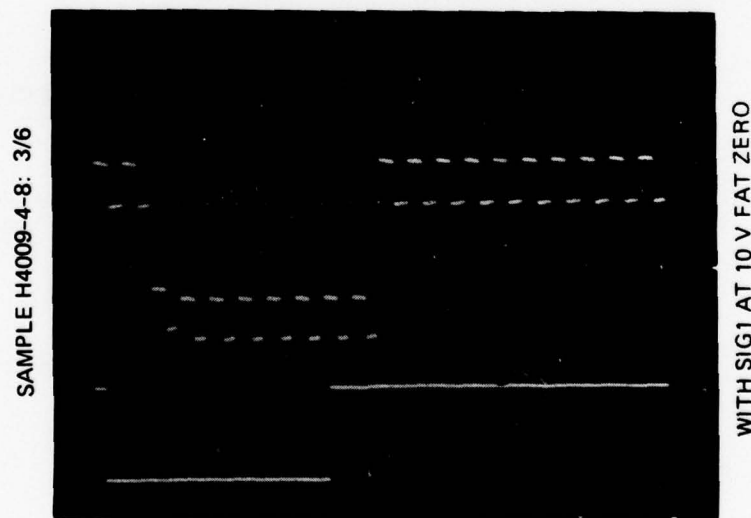


Figure 18. Serial SCCD input register testing: timing waveforms for MASC SIR testing (SIG waveforms are for loading scheme No. 3).

responsible for the transfer inefficiency in SCCDs. To avoid this problem, clock voltages, which do not accumulate holes at the surface during the off phase of each cycle, can be used. In effect, this biasing scheme toggles the MOS gate between the conditions of partial inversion and deep depletion and thus does not allow the surface states to lose their trapped charge on each clock cycle. Once these states have been initially filled, they no longer need to extract charge from the signal and therefore do not contribute to the overall transfer efficiency. In this operating mode, the fat zero technique is not expected to yield a significant η_T (SCCD) improvement. The fat zero technique (described in Section 3.A) provides a free charge background (or zero level) from which the surface states can supply their charge requirements.

The transfer efficiency results reported on Contract No. DAAG53-76-C-0066 were obtained with the latter clocking scheme (no accumulation). Here we found a relatively small change (from 0.9996 to 0.9998) with the inclusion of a fat zero. For experiments on this program, we used the above accumulation-mode clocking scheme in conjunction with the fat-zero technique to illustrate dramatically the effects of surface state traps on transfer efficiency. The effect of fat zero are clearly shown in Figure 19, where η_T changes from 0.997 to 0.9997 with the incorporation of a large (~40%) fat zero. The total effect of the SCCD transfer efficiency for a particular device can be seen from the ratio between the first and second output data bits following a string of empty buckets. This, in conjunction with Eq. 1, can be used to provide a numerical value for η_T . The above data are typical and represent the mean values for those respective quantities for a series of measurements on at least nine different devices from as many as three different wafers. In addition, exactly the same value of 0.997 was measured for η_T (no fat zero) on the 16-bit LGTTD. The dependence of η_T on the clock repetition frequency is shown in Figure 20, where, for convenience, the transfer inefficiency ($\epsilon_T = 1 - \eta_T$) is plotted. These data show that, above 40 kHz clock frequencies, the η_T (SCCD), with accumulation mode clocking, continuously degrades with increased frequency while no apparent degradation of η_T (SCCD) without accumulation mode clocking is observed. This evidence further supports the role played by surface

LOAD PULSEWIDTH = 6 BITS (600 μ SEC)a) WITHOUT FAT ZERO: $\eta_T = 0.997$ 

LOAD SCHEME NO. 5

b) WITH 40 % FAT ZERO: $\eta_T = 0.9997$

Figure 19. The effect of a fat zero on the SCCD serial input register charge transfer efficiency. Accumulation mode (10 kHz) clocking used in both cases.

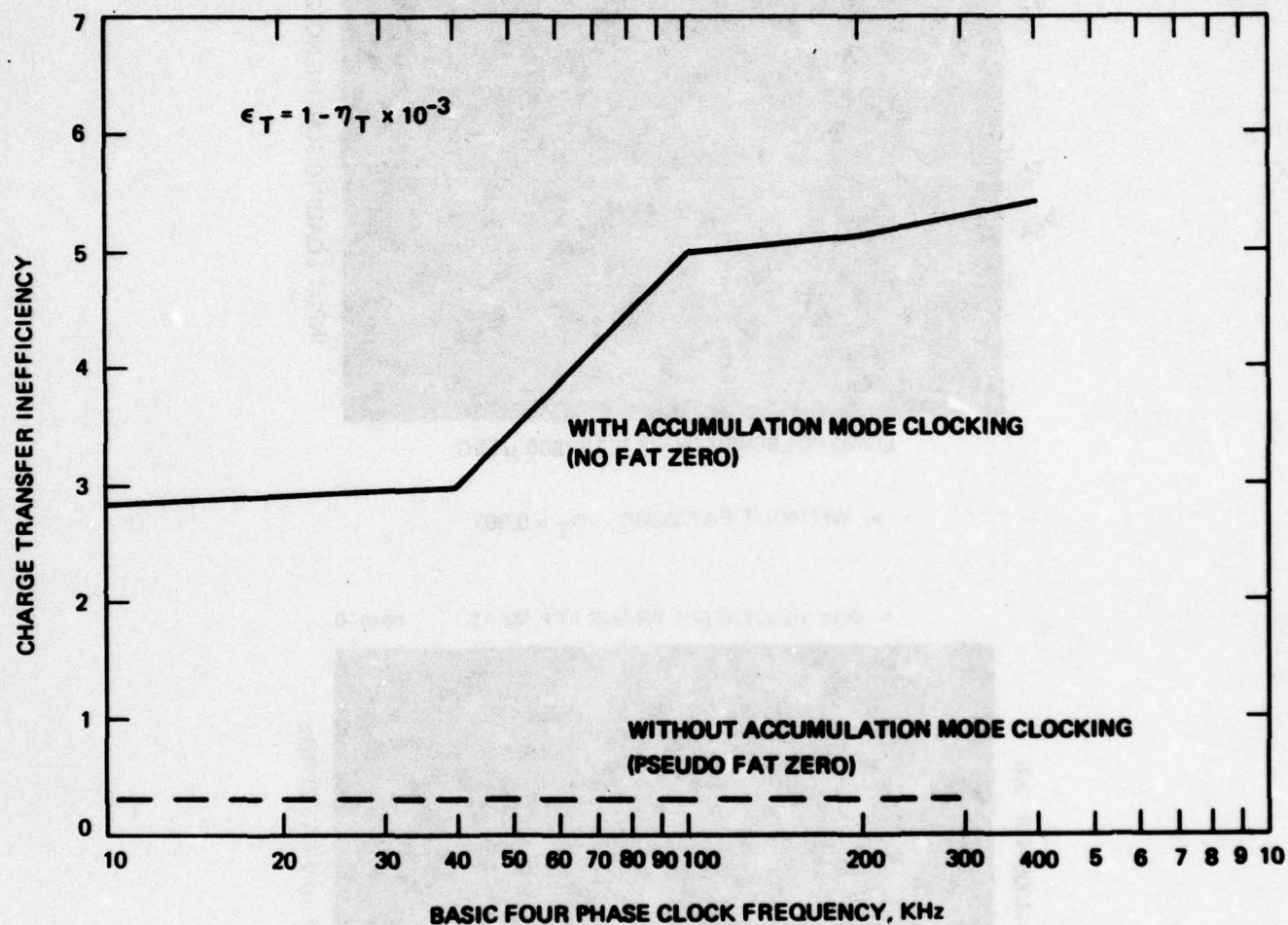


Figure 20. Frequency dependence of SCCD transfer inefficiency ($\epsilon_T = 1 - \phi_T$) of the 65-bit serial input register.

states in determining both the numerical value of the SCCD ϕ_T and its dependence on clock frequency. Hence, during the fabrication of any future CCD LCLV substrates, careful attention must be paid to the CCD gate oxidation process to minimize the interface state density.

Several alternative loading schemes were investigated on the SCCD serial input register to determine the configuration that would maximize linearity between analog signal input and output. The three major loading schemes studied here are described in Table 1, and the SCCD SIR input structure and the associated nomenclature appropriate for this device are shown schematically in Figure 17. The three schemes used here differ primarily with respect to which serial input gate (SIG) is used to introduce the analog signal and whether these data are represented by a fixed dc voltage or as the amplitude of a turn ON (depletion) pulse. The observed input/output (I/O) signal relations for each of these loading methods are shown in Figures 21 through 23. In the standard "fill and spill" loading scheme (LS1), in which a dc voltage is used on gates SIG2 and 3, the observed transfer characteristic is only linear over a limited range of input signal voltages (approximately 6 to 8 V). Below this linear region, there is no output signal; above it, the output signal amplitude saturates. The maximum deviation from linearity for $6.5 \text{ V} \leq \text{SIG}_{2,3} \leq 8.0 \text{ V}$ is $\sim 2.1\%$. The existence of these threshold and saturating characteristics is not an artifact of the SCCD output charge amplifier because similar behavior was observed in the measurements described in Section 3.A on the LGTTD. There the output signal charge for both the BCCD and the SCCD registers was measured directly with an external amplifier/integrator arrangement and yet the same threshold/saturation transfer characteristic for both the BCCD and the SCCD structures was observed for this particular input loading scheme (LS1).

The transfer characteristic for loading scheme 2 (LS2) is shown in Figure 22. In this mode of operation, the input data resides on SIG1, where a dc voltage proportional to the analog signal is applied.

Table 1. SCCD Alternative Input Loading Scheme Studied

Loading Scheme No.	Input Diode	SIG ^a 1	SIG ^a 2	SIG ^a 3	ϕ_{S1} and ϕ_{S2} for Cell No. 1
LS1	Fill and spill	1. Continuously ON during SIR loading 2. Fixed amplitude	1. Variable amplitude dc proportional to the analog input signal	1. Variable amplitude dc proportional to the analog input signal	1. ON during input diode fill pulse
LS2	Fill and spill	1. Continuously ON during SIR loading 2. Analog signal input proportional to amplitude	1. Fixed amplitude pulse 2. ON during ID pulse 3. OFF after $\phi_{S1}, S2$ turned ON	1. Fixed amplitude pulse 2. ON during ID pulse 3. OFF after $\phi_{S1}, S2$ turned ON	1. OFF during ID pulse 2. ON before SIG2 and SIG3 turn OFF
LS3	Fill and spill	1. Continuously ON during SIR loading 2. Fixed amplitude	1. ON during ID pulse 2. Pulse amplitude proportional to analog input signal	1. ON during ID pulse 2. Pulse amplitude proportional to analog input signal	1. OFF during ID pulse 2. ON before SIG2 and SIG3 turn OFF
^a SIG = serial input gate.					

6596

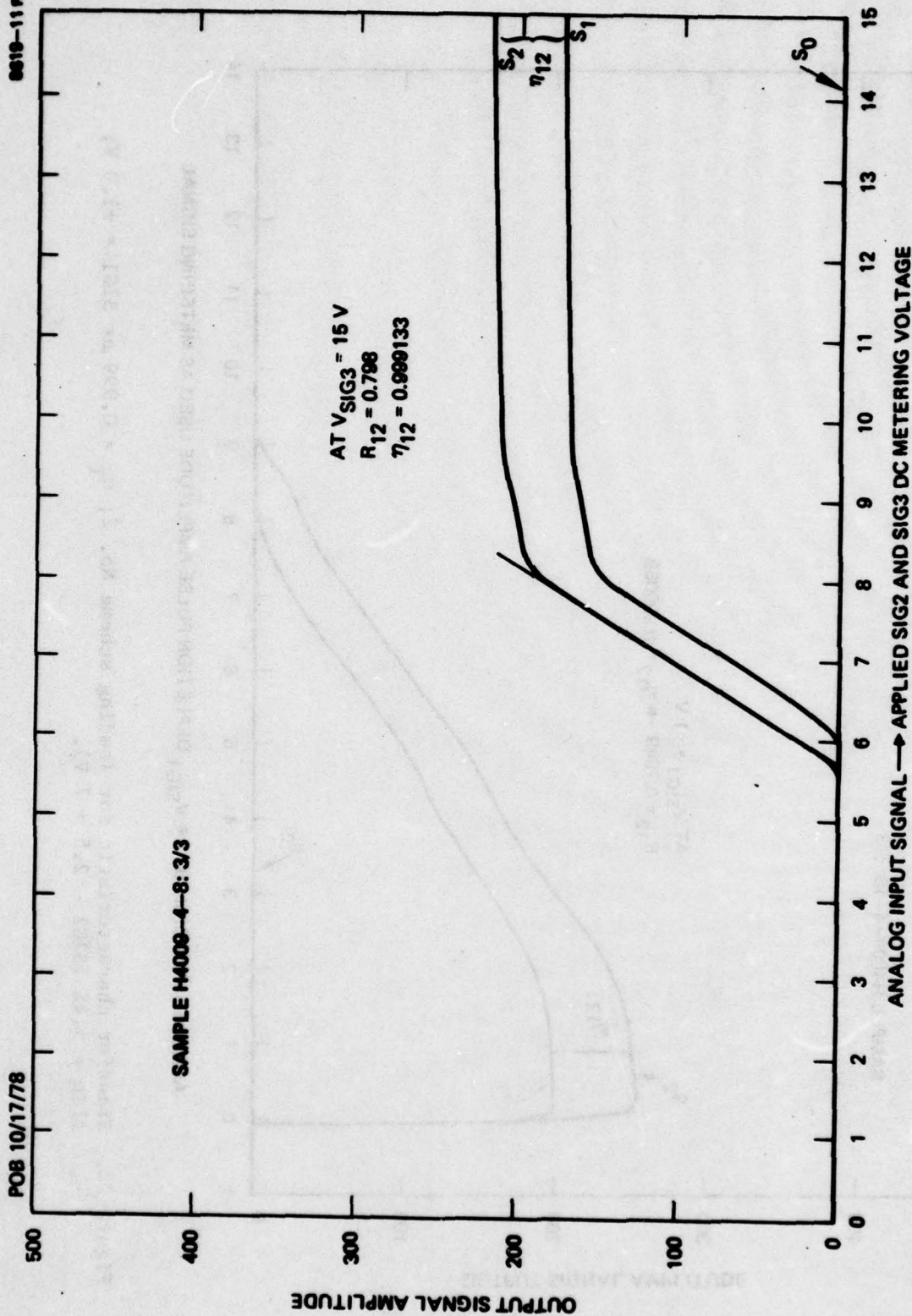


Figure 21. Output signal amplitude as a function of analog input voltage for loading scheme 1. Lower curve is for the first output signal bit, while upper curve represents the second bit of output data. (Clock frequency is 10 kHz. Transfer characteristic of loading scheme No. 1; $\phi_T = 0.999$ at $SIG2 = SIG3 = +15.0\text{ V}$ (ΔLin)_{max} = 2.1% (6.5 → 8.0 V)).

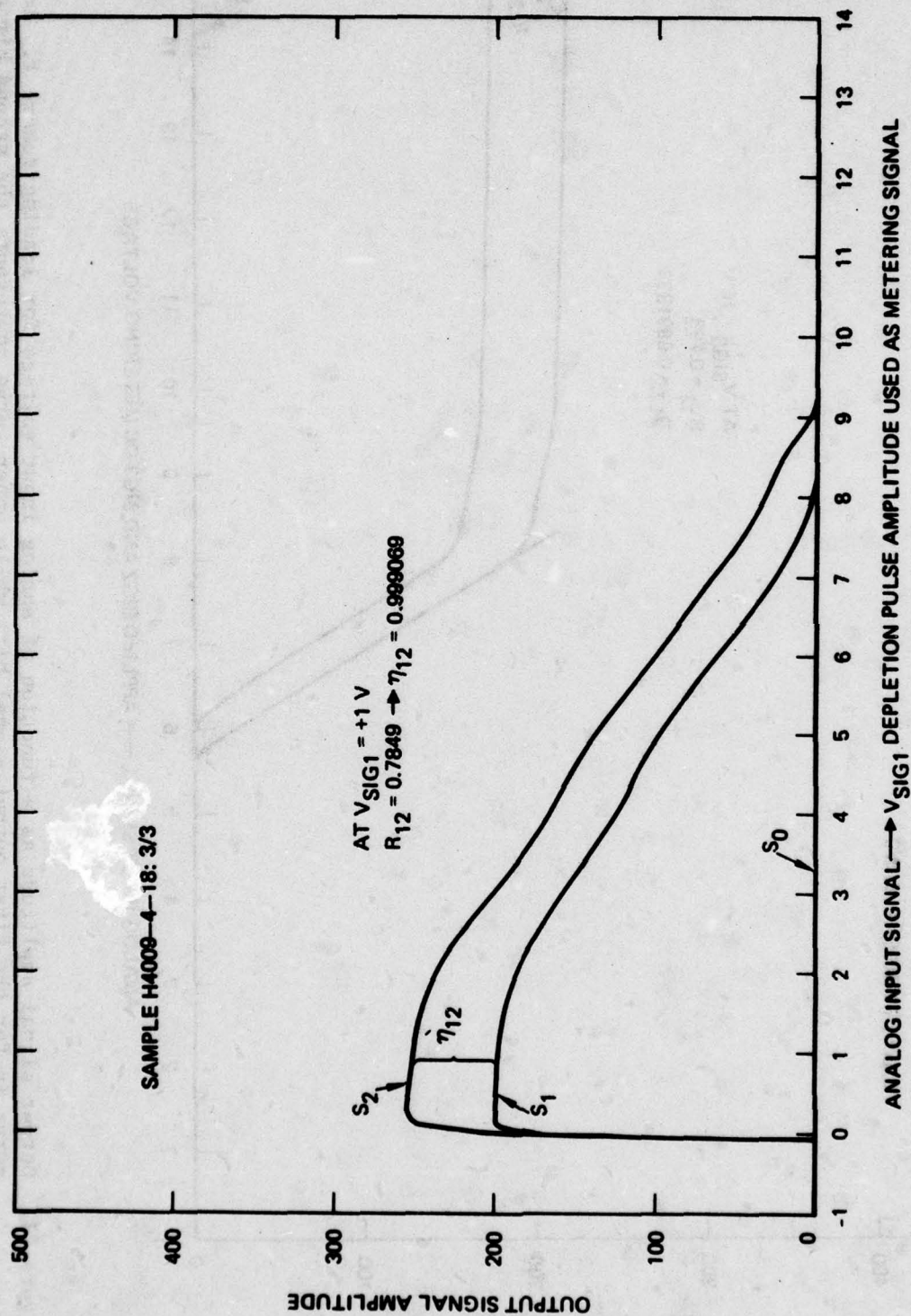


Figure 22. Transfer characteristic for loading scheme No. 2; $\eta_T = 0.999$ at $SIG1 = +1.0\text{ V}$; $\Delta I_{in} = 5.4\%$ ($SIG1 - 2.5 \rightarrow 7\text{ V}$).

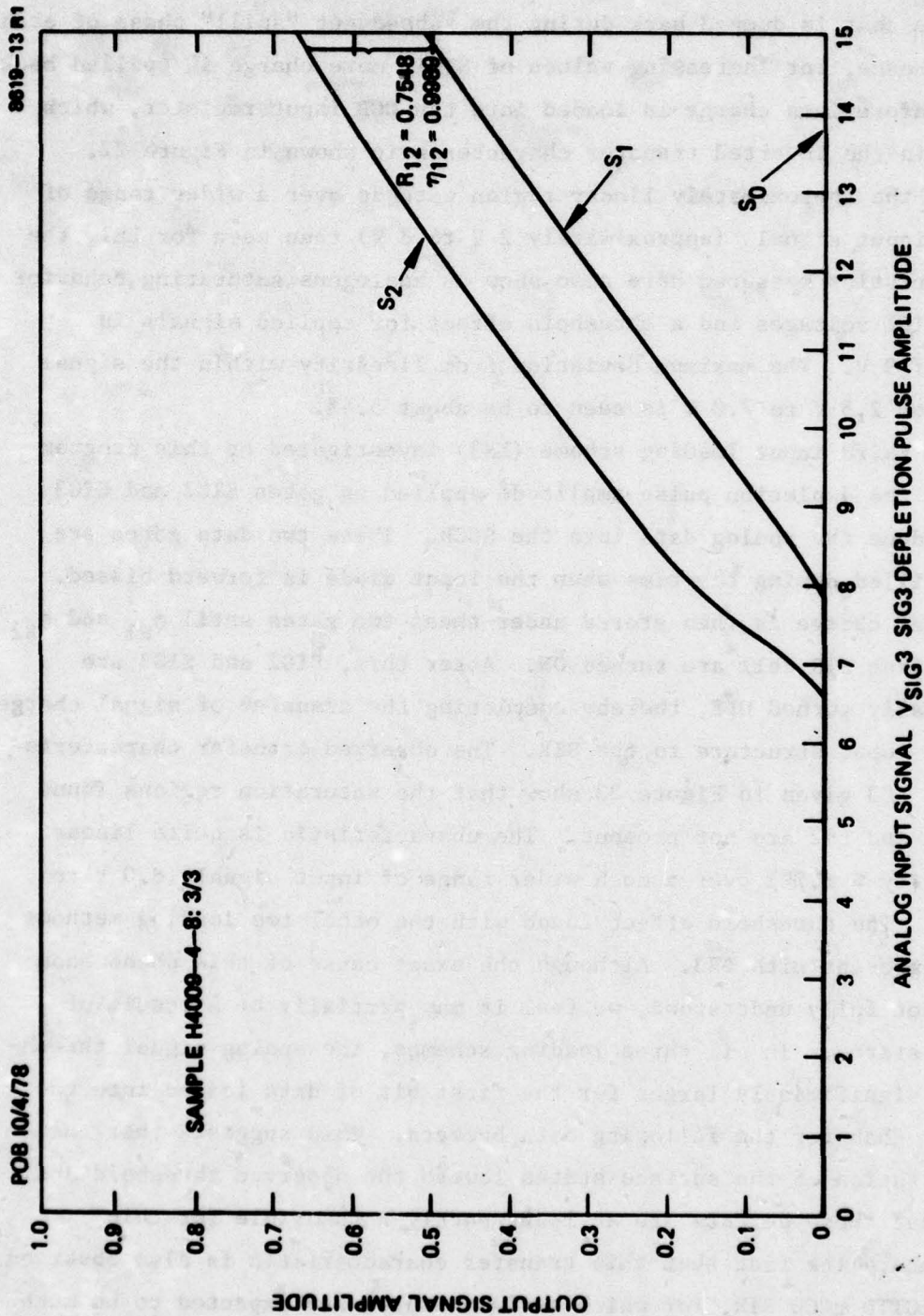


Figure 23. Transfer characteristic for loading scheme No. 3; $\eta_T = 0.999$ at $SIG2 = SIG3 = +5.0$ V (pulsed); $(\Delta Lin) = 1.7\%$ (8.5 V \rightarrow 15.0 V).

The potential on this gate acts both to forward bias the input diode during the "fill" phase of the loading cycle and to determine the amount of charge that is dumped back during the subsequent "spill" phase of each cycle. Hence, for increasing values of SIG1, more charge is spilled back and therefore less charge is loaded into the CCD input register, which results in the inverted transfer characteristic shown in Figure 22. Although the approximately linear region extends over a wider range of applied input signal (approximately 2 V to 8 V) than seen for LS1, the characteristics measured here also show an analogous saturating behavior at low SIG1 voltages and a threshold effect for applied signals in excess of 9 V. The maximum deviation from linearity within the signal range from 2.5 V to 7.0 V is seen to be about 5.4%.

The third input loading scheme (LS3) investigated on this program utilizes the depletion pulse amplitude applied on gates SIG2 and SIG3 to introduce the analog data into the SCCD. These two data gates are ON and filled during the time when the input diode is forward biased. The signal charge is then stored under these two gates until ϕ_{S1} and ϕ_{S2} of the first SIR cell are turned ON. After this, SIG2 and SIG3 are sequentially turned OFF, thereby completing the transfer of signal charge from the input structure to the SIR. The observed transfer characteristics for LS3 given in Figure 23 show that the saturation regions found with LS1 and LS2 are not present. The characteristic is quite linear ($\Delta\text{linearity} \leq 1.7\%$) over a much wider range of input signal (8.0 V to 15.0 V). The threshold effect found with the other two loading methods is also present with LS3. Although the exact cause of this phenomenon is not yet fully understood, we feel it may partially be a result of surface states. In all three loading schemes, the analog signal threshold was significantly larger for the first bit of data loaded into the register than for the following data buckets. This suggests that the neutralization of the surface states lowers the observed threshold and hence that these defects are at least partly responsible for this phenomenon. The fact that this transfer characteristic is also observed on the LGTTD BCCD SIR, for which surface states are expected to be much less important, suggests that several different mechanisms may be

responsible for this effect. Since, as shown by both the η_T and transfer characteristic measurements, the surface states at the Si/SiO₂ interface significantly degrade performance, we suggest that careful attention should be paid to minimizing the incorporation of these defects in any future CCD CLCV substrate fabrication runs.

SECTION 4

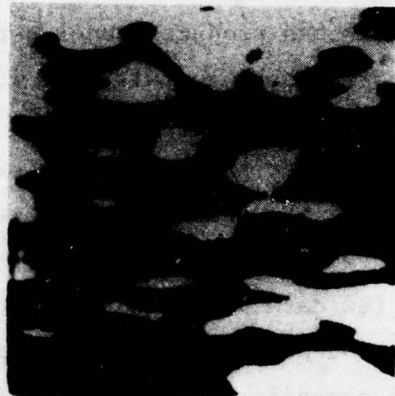
ELECTRICAL AND OPTICAL EVALUATION OF CCD LVs

A primary goal of this contract was to test and evaluate CCD LVs fabricated from wafers that had been produced under a previous contract. This section describes the results obtained with the 16 CCD LVs fabricated as part of this contract. The purpose of this effort was to fabricate the best possible CCD LV at this stage, to evaluate the performance of the present design of the readout structure, and to recommend improvements on the original design. Prior to this, only a few CCD LVs had been fabricated and thus few data were available for making this evaluation. Of these, only one demonstrated any optical modulation, and this was very limited and nonuniform (see Figure 24). No spatial resolution was observed. Improvements in the mirror deposition method produced high and uniform output light modulation (50:1 contrast ratio), as shown in Figure 25. We were also able to demonstrate the feasibility of a conversion from serial electrical to parallel optical which includes resolution. (The optical resolution was capable of 13 lines across the device. Thus, one optical resolution line corresponds to 5 CCD lines.) To give a complete summary of the performance level of the device, we will necessarily also have to include information generated as a result of our IR&D efforts.

A. ELECTRICAL EVALUATION OF READOUT STRUCTURES

The two key parameters of the readout structure are the minority carrier lifetime and the charge transfer efficiency from the CCD through the wafer to the readout MOS. The minority carrier lifetime is important because we are limited by the time required to fill the CCD parallel array to a frame time of ~ 25 msec. Thus, the depletion region must not collapse during this time. To prevent its collapse, the thermally generated current must be kept within the region $\leq 0.1 \mu\text{A}/\text{cm}^2$. This current is inversely proportional to the minority carrier lifetime (τ). To achieve the goal of $0.1 \mu\text{A}/\text{cm}^2$, τ must be greater than or equal to 100 μsec . We have found that several things severely degrade the

6504-13



SIGNAL OFF

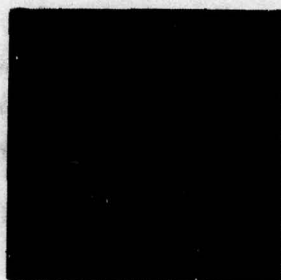


SIGNAL ON

Figure 24.
Prior art photograph of the display
screen on which is focused the CCD
LCLV read out laser beam.

7538-1

OFF



PARTIALLY
ON



FULLY
ON

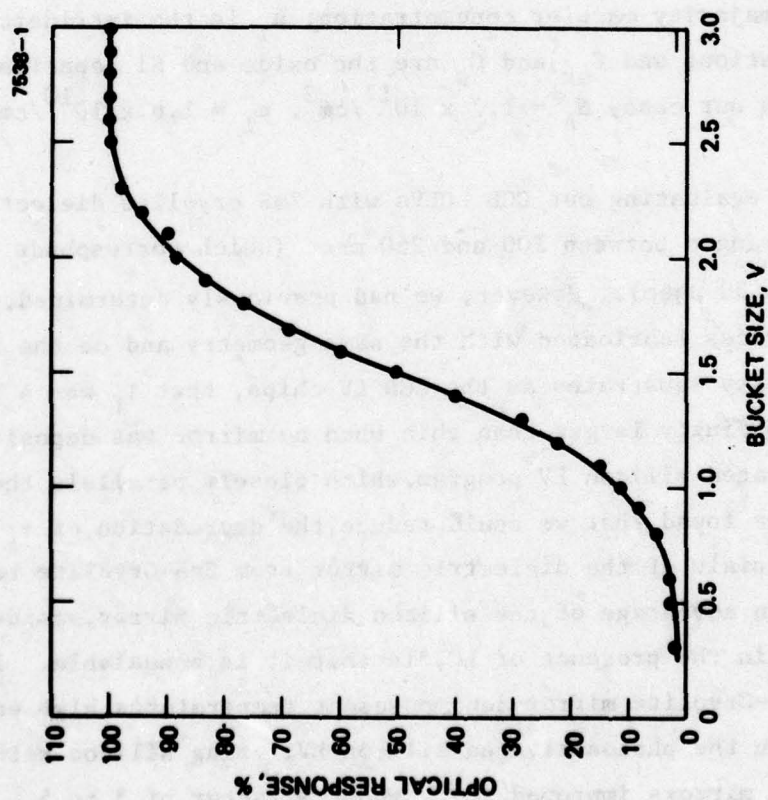


Figure 25. Electrical to optical transfer function of an improved CCD LCLV.

minority carrier lifetime, the most important of which are (1) high-temperature processing and (2) damage from radiation and strain introduced by the deposition of the thin-film LV layers. To probe the degradation caused by the deposition of the LV thin films, a cermet for optical isolation and a dielectric mirror for high optical reflectivity, we made capacitance versus time (C-T) measurements. An example of a typical C-T curve is shown in Figure 26. These data, which were taken on a fully processed LV that had been assembled with LC, show the formation of the depletion region and its subsequent collapse due to thermal generation to the inversion capacitance. The salient feature of the data is the time (known as the transient fill time, τ_f) it takes for the depletion capacitance to increase to the inversion capacitance; τ_f is related to the minority carrier lifetime, τ_G , by

$$\tau_f = \frac{C_{ox}}{C_s} \frac{N_A}{2n_i} \tau_G ,$$

where N_A is the majority carrier concentration; n_i is the intrinsic carrier concentration; and C_{ox} and C_s are the oxide and Si capacitances, respectively. In our case, $N_A = 1.7 \times 10^{12}/\text{cm}^3$, $n_i = 1.6 \times 10^{10}/\text{cm}^3$, and $C_{ox}/C_s \sim 10^2$.

We found in evaluating our CCD LCLVs with ZnS cryolite dielectric mirrors that τ_f ranged between 100 and 250 msec (which corresponds to a lifetime of 20 to 50 μsec). However, we had previously determined, on surrogate MOS devices fabricated with the same geometry and on the similar high-resistivity substrates as the CCD LV chips, that τ_f was 4 to 10 times correspondingly larger than this when no mirror was deposited. In the photoactivated silicon LV program, which closely parallels the CCD LV program, we found that we could reduce the degradation of τ_f by changing the materials of the dielectric mirror from ZnS-Cryolite to Si/SiO₂. The main advantage of the silicon dielectric mirror, aside from better stability in the presence of LC, is that it is annealable. In contrast, the ZnS-Cryolite mirror decomposes at temperatures high enough for annealing. In the photoactivated silicon LV, using silicon rather than ZnS-Cryolite mirrors improved τ_f by about a factor of 3 to 5. The

one experiment with the Si/SiO₂ mirror that we could perform on the present contract did not produce the expected result. We found that τ_f decreased by a factor of 5 to 10, to ~ 20 msec (Figure 27).

This surprising result may be due to the annealing temperature being too low: we had reduced it because of the aluminum contacts on the CCD device (contacts not present in the photoactivated device). The lower temperature, however, did not reduce the damage incurred during the deposition of the cermet and the dielectric mirror. We plan to investigate this anomalous result using a set of surrogate MOS devices (with silicon mirrors deposited on them) to evaluate different annealing conditions.

8619-14

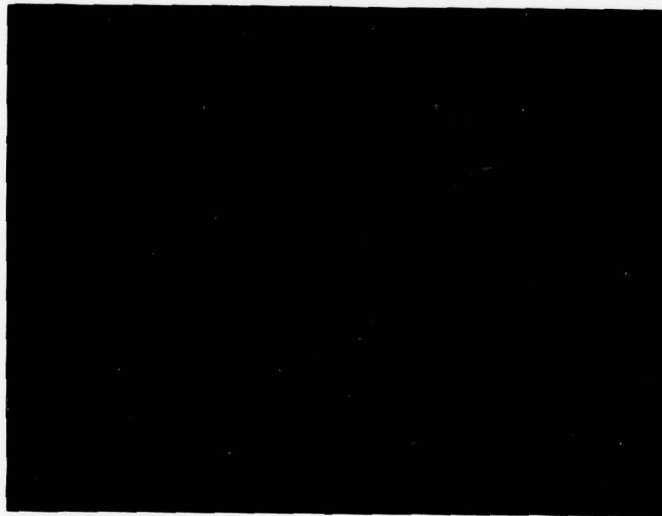


Figure 26.
C-T data on a fully processed CCD LCLV with a ZnS-Cryolite dielectric mirror. Vertical sensitivity is 10 pF/div.; horizontal sensitivity is 20 msec/div. The left graticule mark coincides with the transition from 10 V of accumulation to 20 V of depletion. The transient fill time, τ_f , is 170 msec.

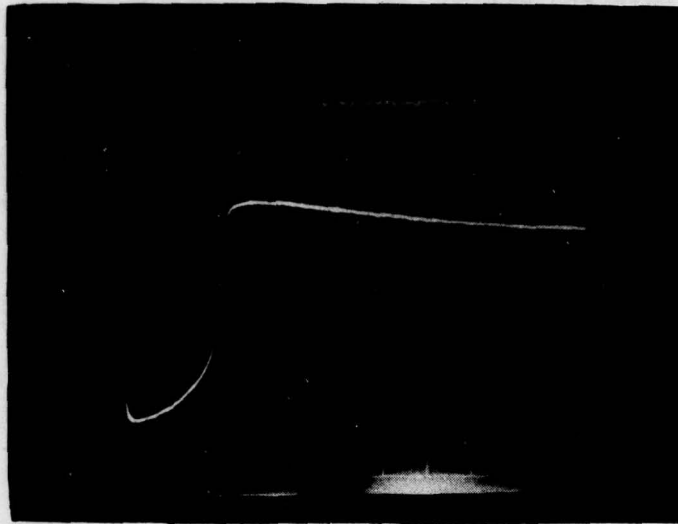


Figure 27.

C-T data on fully processed CCDLV with silicon mirror. Vertical sensitivity is 20 pF/div.; horizontal sensitivity is 5 msec/div. The leftmost graticule mark coincides with the transition from 10 V of accumulation to 20 V of depletion. The transient fill time, τ_f , is 12 msec.

The second key parameter of the readout structure is the efficiency of the transfer of signal charge from the CCD to the readout MOS structure. Before the start of this contract, we were able to demonstrate only partial ability to make this charge transfer to the readout structure (Figure 24) without spatial resolution. By improving the chip dicing procedure and mirror deposition method, we were able to demonstrate high contrast (50:1) and uniform modulation (Figure 25); indeed, we were able to demonstrate some optical resolution. The best optical resolution we obtained was a minimum optical linewidth corresponding to ~ 5 CCD lines. In addition, in operating the CCD LV, we observed an anomalous saturation effect in the amount of signal charge that could be transferred to the readout structure. Work directed at quantifying and understanding these limitations (in order to eliminate them) was partly supported by this contract and partly by our IR&D.

The testing procedure consisted of completely filling the CCD parallel array, so that the signal charge is stored in the "buckets" formed under the ϕ_4 clock gates. The adjacent clock gates are held at a low voltage (producing a high potential hill for the signal electrons) while the voltage on the storage gate, ϕ_4 , is ramped down, releasing the signal electrons. The ϕ_4 gate voltage is ramped down rather than abruptly lowered to avoid producing high currents and suffering their attendant effects.

To evaluate carefully the signal charge transfer from the CCD to the readout MOS, the device should operate in the simplest manner possible — as if the entire parallel array was one single CCD element (one MOS capacitor). The principal chip components, the electrical test setup, and the waveforms are shown in Figure 28. The clock gates of the serial surface channel CCD are electrically tied to the transfer gate. This assembly of gates is then used as an ON-OFF gate to allow charge from the input diode to flow into the parallel CCD array. The width of the ON time determines the parallel array loading time. Just before turning on this assembly of gates (called the transfer gates), the voltage on the parallel array gates (all four clock phase gates are tied together) is turned on to form the charge "bucket." Thus, the voltage on these gates determines the depth of the bucket and the amount of signal charge to be dumped to the readout structure. Just before dumping the signal charge from the CCD parallel array, the LC power supply quickly accumulates the readout MOS and then depletes it. The voltage on the CCD parallel array is ramped down, rather than simply turned off, to dump the signal charge out slowly and avoid high currents in the epi.

Figure 29 shows typical data illustrating the saturation of signal charge transfer to the readout MOS. The upper trace on each of the data photographs is the voltage on the CCD parallel array gates (i.e., the bucket size). The middle trace is for the transfer gates and the lower trace is of the current supplied by the LC power supply to match the signal charge transferred to the readout MOS. On all of the photographs, the current pulse, observed immediately after the transfer gates are

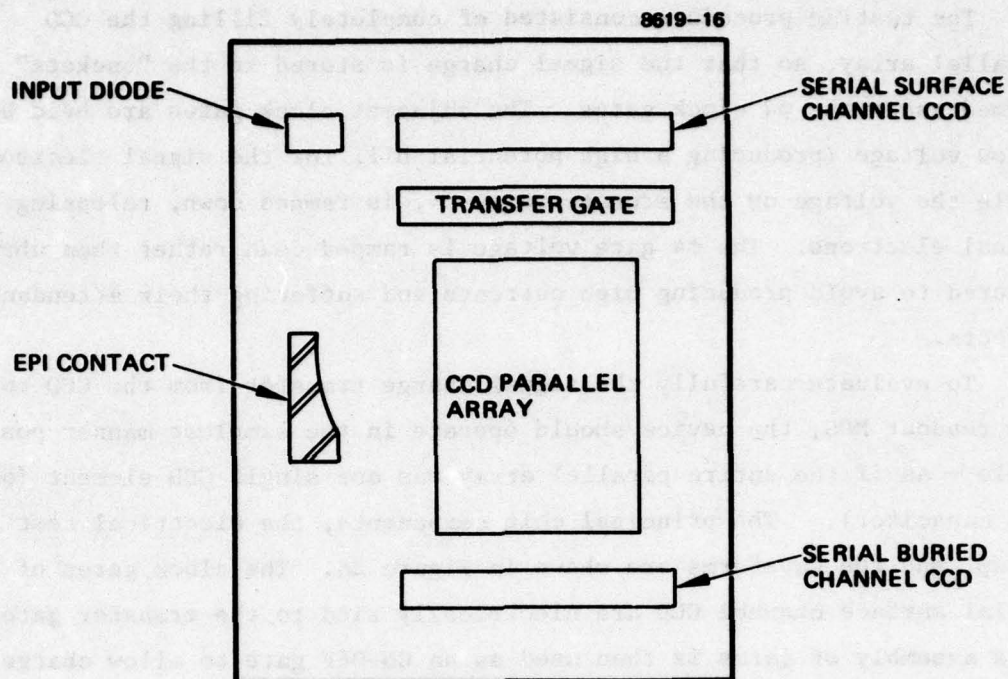


Figure 28(a). Top view of CCD chip.

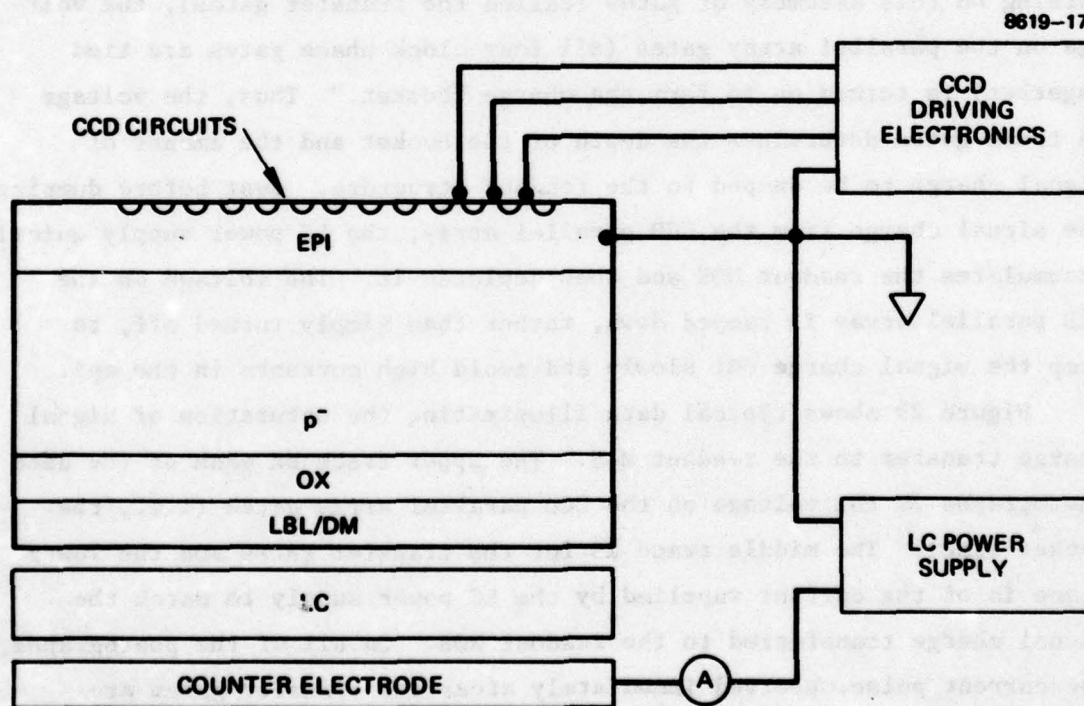


Figure 28(b). Cross-sectional view of CCD LCLV.

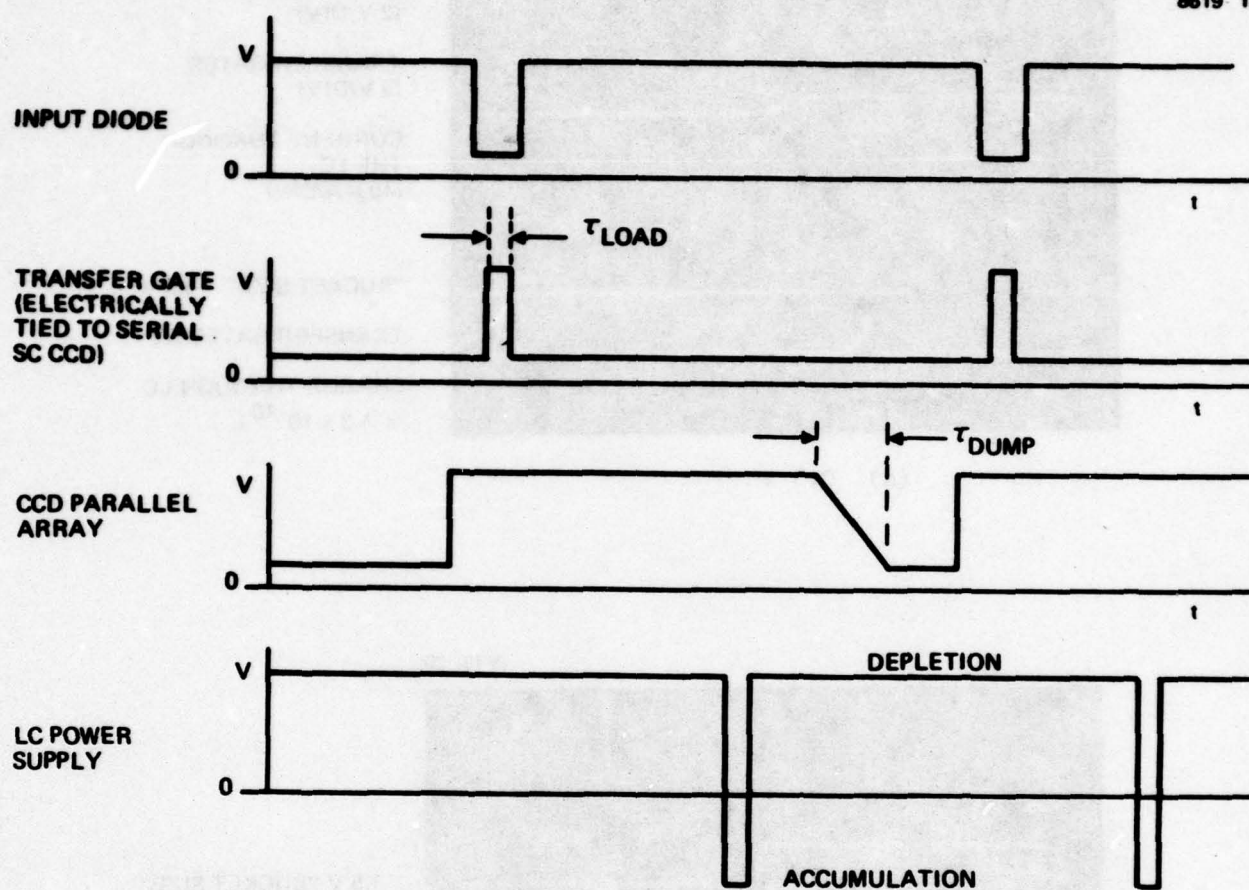
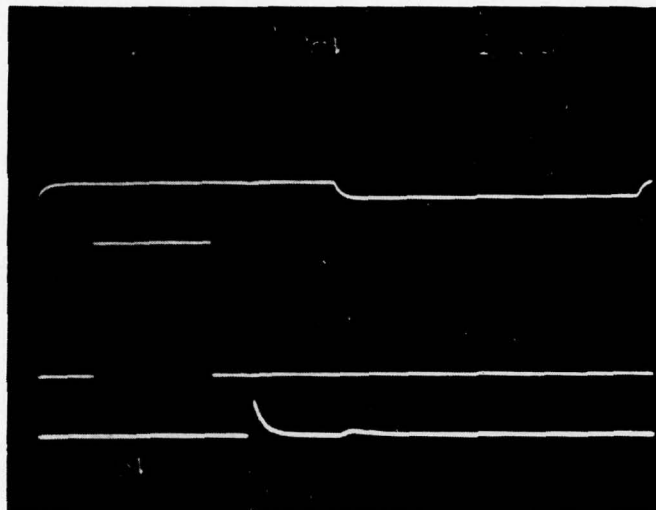


Figure 28(c). Waveforms and timing of experimental signals.

8619-19



VOLTAGE ON
PARALLEL ARRAY
CLOCK GATES
(2 V/DIV)

TRANSFER GATES
(5 V/DIV)

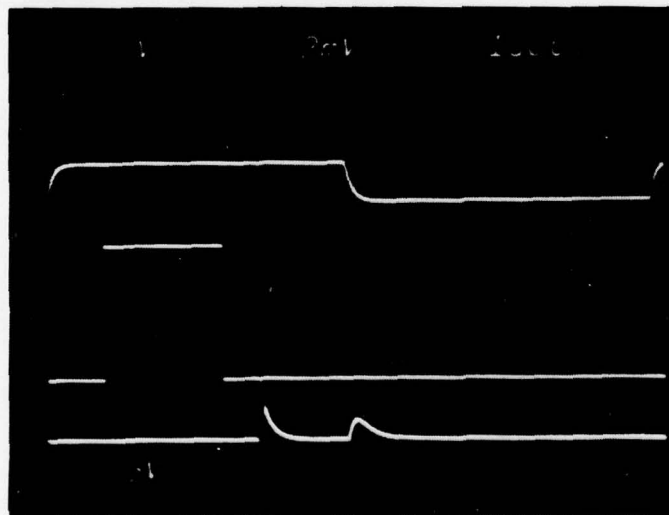
CURRENT THROUGH
THE LC
(40 μ A/DIV)

"BUCKET SIZE" 0.5 V

TRANSFER GATES ON
CHARGE THROUGH LC
 $\approx 1.3 \times 10^{-10}$ C

(a) 0.5 V

8619-20



1.5 V "BUCKET SIZE"

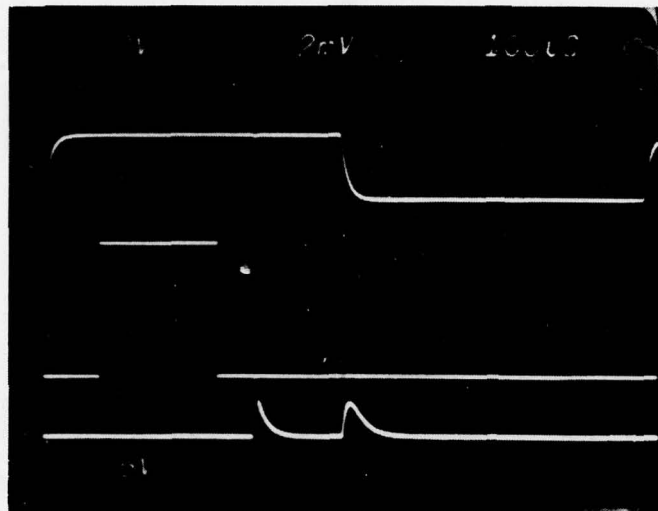
TRANSFER GATES ON

CHARGE THROUGH LC
 $\approx 7.5 \times 10^{-9}$ C

(b) 1.5 V

Figure 29. Typical data showing the saturation of signal charge transfer to the readout MOS for various "bucket sizes."

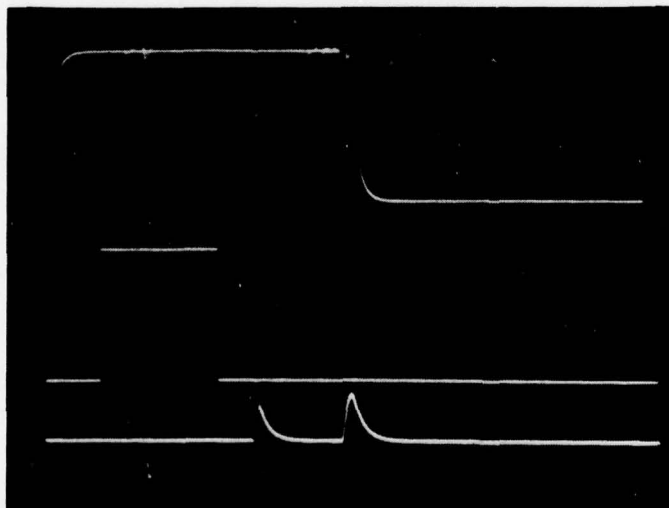
8619-21



2 V "BUCKET SIZE"
TRANSFER GATES ON
CHARGE THROUGH LC
 $\approx 1.1 \times 10^{-9} \text{ C}$

(c) 2 V

8619-22

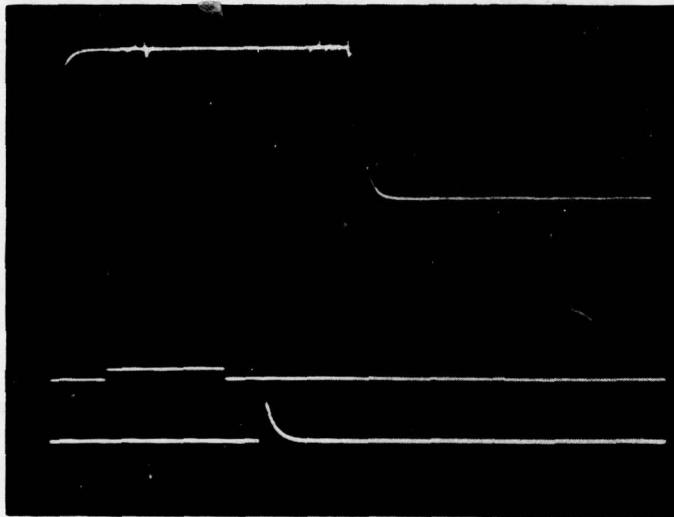


5 V "BUCKET SIZE"
TRANSFER GATES ON
CHARGE THROUGH LC
 $\approx 1.2 \times 10^{-9} \text{ C}$

(d) 5 V

Figure 29. Continued.

8619-23



5 V "BUCKET SIZE"

TRANSFER GATES OFF

CHARGE THROUGH LC

≈ 0

(e) 5 V (but with the transfer gate turned off).

Figure 29. Continued.

turned OFF, is an artifact of the narrow accumulation pulse. In Figure 29, the transfer gates are left OFF and the accumulation pulse artifact remains but the LC current is zero. The arrival charge in the LC circuit appears coincident with the dumping of charge from the CCD parallel array. The increase in charge through the LC is approximately linear with increasing "bucket size" up to ~ 2 V. Beyond ~ 2 V the charge through the LC does not increase to any appreciable extent, as Figure 29(d) shows.

A second set of experiments was done to ensure that the full amount of signal charge was going into the CCD parallel array. A modified experimental test setup was used (see Figure 30) to measure the amount of charge injected from the input diode into the CCD parallel array while simultaneously looking at the current (i.e., the charge) in the LC power supply circuit. Since the difference in the amount of charge injected from the input diode and that collected in the readout MOS must appear in the epi, the current in the epi was also monitored. Typical results of this type of experiment are shown in Figure 31. The observed quantity of charge injected from the input diode is 1×10^{-8} C for a 15-V "bucket size;" the calculated "bucket size" is 2.2×10^{-8} C. The charge through the LC with a 15 V "bucket size" is as it had been with the 2 V "bucket size" (Figure 29(c), $\sim 1 \times 10^{-9}$ C. Figure 31(c) shows the current in the epitaxial layer. The positive (upward-going) current pulse is due to the displacement of majority carriers when the CCD parallel array "buckets" are formed. The negative-going current pulse, which is coincident with the dumping of the signal charge, is measured to be $\sim 1 \times 10^{-8}$ C. Thus, we definitely have full "buckets" but at the full saturation level, only $\sim 10\%$ of the signal charge is transferred to the LC.

This saturation effect may be due to dumping too much charge into the readout MOS (i.e., too much signal). We have demonstrated that a 2-V "bucket size" is enough to achieve 90% of the liquid crystal response (see Figure 27). This demonstrates that, as far as the signal strength is concerned, we have a significant factor, some of which can be traded for better performance in other areas. Charge is transferred to the readout structure while the high resistivity bulk is depleted. Using

the parameter values shown in Table 2 and the equivalent circuits shown in Figure 32, we calculate that the charge required to collapse the depletion layer completely is $\sim 3.4 \times 10^{-9}$ C. This number is in reasonable agreement with the maximum quantity of charge observed in the LC circuit, 1×10^{-9} C.

This saturation effect, which appears at approximately a 2-V bucket size when all the CCD parallel array clock gates are tied together, is not expected to appear until ~ 6 V, when the device is operating in the intended CCD mode. This is because, with all the gates tied together, charge is stored under all the clock gates; but, when operating in the CCD mode, charge is stored only under one of the gates, ϕ_4 , which occupies $\sim 1/3$ of the cell size. (The effective widths of ϕ_1 and ϕ_3 clock gates are ~ 0.2 mils each, while the widths of gates ϕ_2 and ϕ_4 are ~ 0.5 mils each). Typically, we have operated the CCD LCLVs with "bucket sizes" ranging from 5 to 8 V. We did not have an opportunity to test this hypothesis experimentally before the end of the contract, but we intend to do so in the very near future.

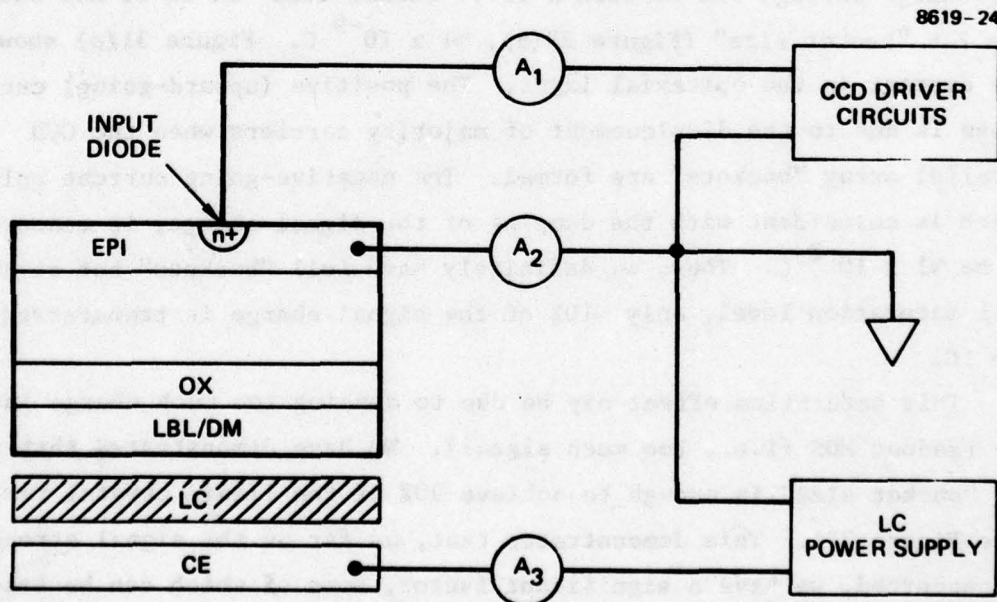


Figure 30. Modified experimental test schematic.

8619-25



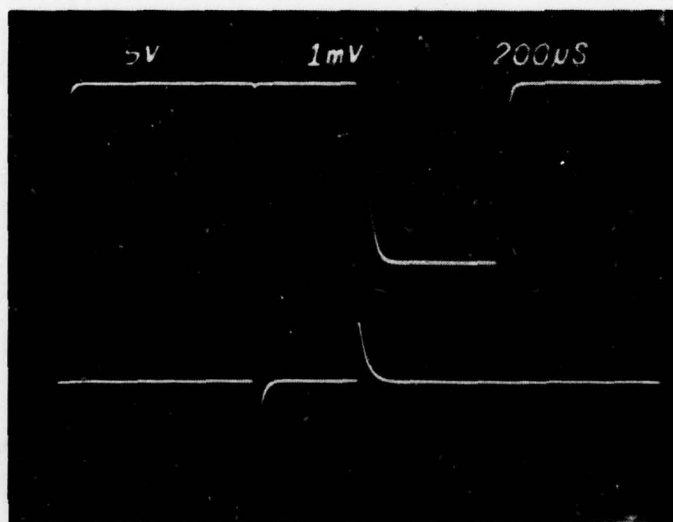
CURRENT SUPPLIED BY
THE INPUT DIODE
(50 μ A/DIV)

$\rightarrow Q_{\text{INPUT}} \approx 1 \times 10^{-8} \text{ C}$

VOLTAGE ON TRANSFER
GATES
(5 V/DIV)

(a) The time dependence of current supplied by the input diode

8619-26



VOLTAGE ON CCD
PARALLEL ARRAY GATES
(5 V/DIV)

15 V "BUCKET SIZE"

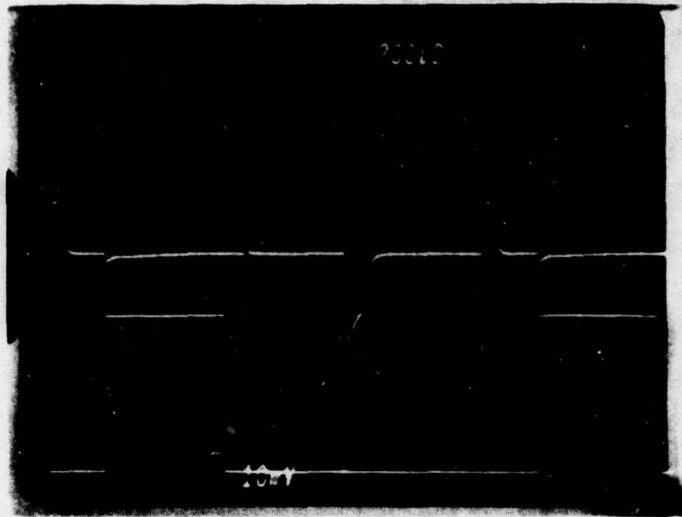
CURRENT THROUGH LC
(20 μ A/DIV)

$\rightarrow Q_{\text{LC}} \approx 1 \times 10^{-9} \text{ C}$

(b) LC power supply current

Figure 31. Typical experimental results.

8619-27



CURRENT THROUGH EPI
TO GROUND
(200 μ A/DIV)

$$\rightarrow Q_{EPI} \approx 1 \times 10^{-8} \text{ C}$$

VOLTAGE ON TRANSFER
GATES
(5 V/DIV)

(c) Epitaxial layer.

Figure 31. Continued.

Table 2. Parameter Values of Read-Out Structure

Read-Out Structure Element	Area, cm ²	Thickness, cm	Dielectric Constant	Capacitance, F
Depletion layer	1.6×10^{-1}	1.2×10^{-2a}	12	1.4×10^{-11}
Oxide	1.6×10^{-1}	1×10^{-5}	4	6.0×10^{-9}
Mirror LBL	1.6×10^{-1}	5×10^{-4}	12	3.5×10^{-10}
Liquid crystal	1.6×10^{-1}	1.5×10^{-4}	4	3.8×10^{-10}

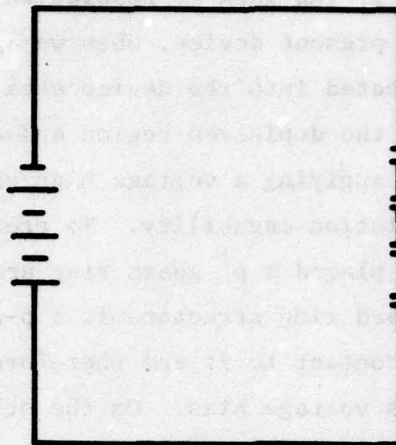
^a20-V depletion voltage.

6596

FULLY DEPLETED

8619 28

LC
POWER
SUPPLY
= 20 V



$C_{\text{DEPLETION LAYER}}$
 C_{OXIDE}
 C_{MIRROR}
 C_{LC}

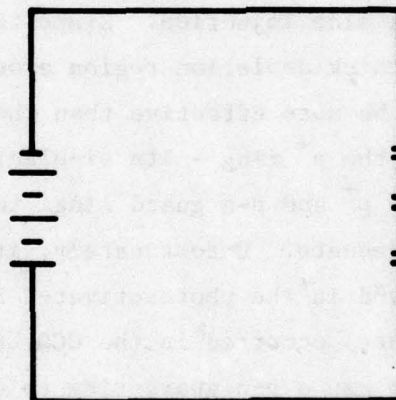
$$C_{\text{TOTAL}} = 1.3 \times 10^{-11} \text{ f}$$

$$Q_{\text{TOTAL}} = CV = 2.5 \times 10^{-10} \text{ C}$$

DEPLETION LAYER COLLAPSED

8619-29

20 V



C_{OXIDE}
 C_{MIRROR}
 C_{LC}

$$C_{\text{TOTAL}} = 1.8 \times 10^{-10} \text{ f}$$

$$Q_{\text{TOTAL}} = 3.6 \times 10^{-9} \text{ C}$$

Figure 32. Equivalent circuit of read-out structure.

The most likely reason for the lack of resolution beyond 5 CCD lines is "side injection." In the present device, when we apply voltage above a certain level, charge is injected into the device area from the periphery, which causes the collapse of the depletion region and a loss of resolution. This effect precludes applying a voltage high enough to achieve full depletion and full resolution capability. To protect the active area from side injection, we placed a p^+ guard ring around the area. An alternative protective guard ring structure is a p-n diode. The p^+ does not require electrical contact to it and therefore is simpler than the p/n diode, which requires voltage bias. On the other hand, the p^+ protects primarily against surface injection, being less effective against bulk injection. The p-n diode guard ring is used in almost all Si devices. When we designed the CCD LCLV, we questioned whether it would be adequate for our device because of the thick depletion region that spreads across the whole thickness of the wafer. The thick depletion region can also collect bulk side injection. Since the biased p-n guard ring creates its own thick depletion region around the active area depletion region, it should be more effective than the p^+ ring. But because of the advantage of the p^+ ring — its simplicity — we decided to design masks for both the p^+ and p-n guard rings to determine if the simpler approach would be adequate. Unfortunately, it is not: the same injection effect observed in the photoactivated Si LCLV (which has an identical readout structure) occurred in the CCD LCLV. With the Si LCLV, it was necessary to use a p-n guard ring to eliminate the injection; the same approach presumably will be effective with the CCD device. And, using the p-n ring with the photoactivated device, we have already achieved resolution corresponding to one CCD line. Therefore, one of our recommendations for the next iteration (which will be the first iteration of the original design) is the implementation of the p-n guard ring in the CCD LCLV.

B. OPTICAL EVALUATION

This section describes the CCD LCLV optical evaluation procedure and the results obtained. To speed up the process, we adopted a staged evaluation procedure. With this approach, the quickest and easiest evaluation is done first. Then, if the device passes this test, the next evaluation stage is undertaken, and so on. This approach minimizes the turnaround time. The three testing stages are:

- Non-CCD optical modulation test (non-CCD OMT)
- CCD optical modulation test
- CCD optical resolution test.

In the non-CCD OMT, all of the CCD parallel array clock gates are electrically tied together in the same manner as much of the electrical evaluation was done. Charge is then loaded into the parallel array and transferred to the LC. This test and all the other optical evaluation tests are done on the optical test bed shown in Figure 33. Then, while the operator observes the screen, the LC power supply voltages, the bucket size voltage, and the timing of the accumulation pulse (with respect to when the signal charge is dumped to the LC) are varied. This stage of the evaluation determines (1) depletion and accumulation voltages appropriate for operation of this device, (2) the electrical to optical transfer relationship (which must be scaled for later use in the CCD mode), and (3) the available contrast with this device. (An example of the electrical to optical transfer relationship is shown above in Figure 25). These data demonstrate a contrast of 50:1, which is typical.

If a device produces no optical modulation, then we must determine if the problem is with the read-out structure or with an inability to introduce charge into the parallel array. This is determined by the results of the next stage of testing.

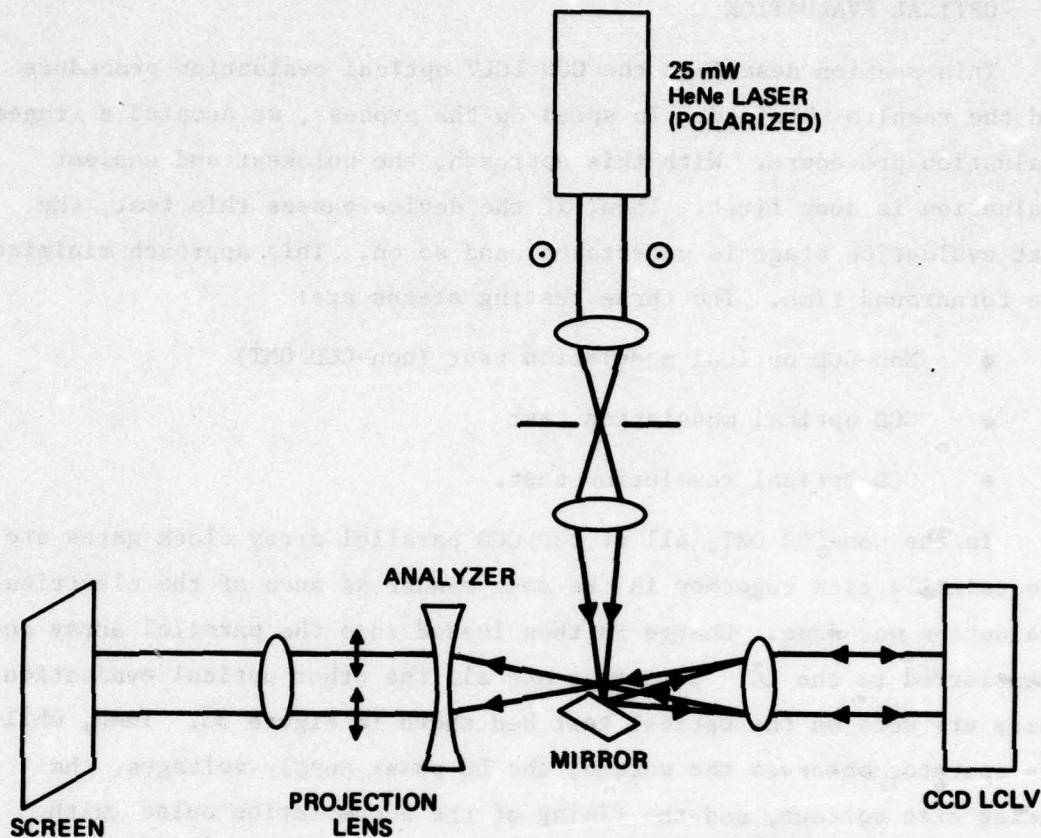


Figure 33. Experimental optical test setup.

The second stage of testing involves setting up the CCD circuits and clocking the signal into the parallel array and then clocking it back out for electrical detection. If successful, this establishes that the CCD circuits are still working properly. But if the CCD circuits cannot be made to work properly and no optical modulation was observed in the first stage, then we can conclude that it was damage to the CCD circuits (incurred during the LV fabrication process) that prevented signal from being loaded into the parallel array. If the CCD circuits work and no optical modulation was observed in stage one, then we conclude the problem is with the read-out structure.

The final test of the CCD LCLV is to modulate the CCD input data to evaluate the resolution capabilities of the device.

Our testing results for this relatively short contract are impressive. Prior to the contract, only 12 CCD LCLVs had been assembled and tested. On this contract, we assembled and tested 16 more; our test results are summarized below:

- 12 of the 16 survived the LV processing with undamaged CCD circuits. This yield of 75% should be compared to our earlier yields of ~30%
- 6 of 16 demonstrated non-CCD optical modulation.
- 2 of 16 demonstrated CCD optical modulation.
- 1 of 16 demonstrated a limiting resolution of 5 CCD lines.

SECTION 5

LIGHT VALVE PROCESSING

Light-valve processing consists of those steps required to convert the CCD silicon chip into an LCLV substrate. The problems encountered in designing and implementing these processing steps arise primarily from the small size of the chip.

The CCD LCLV under development differs significantly from the thin-film light valves that we have developed over the past few years. Those valves typically have an aperture of 25 to 50 mm. The thin-film layers (photoconductor, light-blocking layer, mirror, and LC alignment layer) are deposited onto a thick glass substrate that is both optically flat and mechanically rigid. Since the input information is optical, only two electrical connections are required to supply the audio frequency voltage that activates the LC. By comparison, the CCD LCLV has an aperture of ~ 2 mm. The CCD chip is a thin, flexible substrate that is not optically flat. In addition, these devices require 35 inputs (in the present configuration), 8 of which must operate at 100 MHz. Thus, many of the problems encountered in the two kinds of light valves are quite different.

A closer relative of the CCD LCLV is the silicon photoactivated LCLV that is currently being developed at HRL. Because there are several problems that are common to both devices, each device benefits from progress made on the other. For instance, both LCLVs use essentially identical readout structures that consist of the backside gate oxide on which are deposited the LBL (cermet) and the DM. It is the implementation of this read-out structure that is described as LCLV processing.

LCLV processing begins after the wafer level electrical evaluation of each of the CCD dice. Briefly, the LCLV processing steps are listed below in order:

- Deposition of LBL (cermet) and then DM
- Dicing
- First wire bonding
- Die mounting/flattening
- Die installation in package
- Second wire bonding
- Deposition of LC alignment layer (SiO_x)
- Introduce LC and LV counterelectrodes
- Adjust LV counterelectrode.

This processing sequence significantly improves the throughput and yield of CCD LCLV devices over the previous processing sequence. Details of these processing steps and the improvements they have provided are given below.

1. Deposition of Thin-Film LCLV Layers and Dicing

The thin-film LV layers consist of the cermet LBL and the DM. The cermet LBL prevents the small fraction of the read-out beam that is transmitted by the DM from reaching the photosensitive silicon substrate. The cermet is made up of alternating thin films of metal (Sn) and dielectric (SiO_x). The metal layer is thin enough so that it does not form a continuous conductive sheet that would wipe out the ability to have the spatially varying voltages needed to form an image in the LC. Typically, the cermet LBL has an optical density of ~ 5 . The DM is used to provide high optical reflectivity; it is typically made of $\lambda/4$ thickness of alternating layers of ZnS and Cryolite. When our annealing techniques have been improved, layers of Si and SiO_x will be substituted.

In the original processing scheme, the wafers were first diced by sawing, and then the thin-film LCLV layers were deposited on the selected dice. This sequence was required because the ZnS-Cryolite DM is somewhat hygroscopic and therefore would be attacked by the cooling

water used in the sawing operation. However, this ordering of the steps introduced another problem. In the sawing operation, the wafer must be waxed down to a carrier to hold it in place. After sawing, each die must be removed from the wax separately so as not to lose track of which is which. The individual die must then be scrupulously cleaned; if they are not, the subsequently deposited LCLV layers will not adhere well and will peel off the die. Considerable effort was devoted to the optimization of this cleaning procedure. To order the processing steps and then saw and deposit the LCLV layers forced us to handle the individual die frequently: remove the die from the wax, clean and load into and unload from the thin-film deposition holders. As a result, our yield was low and our throughput was very limited.

From our electrical evaluation studies (described in detail above), we determined that the minority carrier lifetime was reduced by a factor of about 100 by the damage to the substrate caused by sawing. While investigating edge passivation techniques to reduce this damage, we began studying minority carrier lifetime in wafers that were scribed and snapped rather than sawn. We found that minority carrier lifetime was not materially altered by the scribe and snap technique. The fill time increased from 5 msec for the sawn samples to 500 msec for the snapped samples. Another advantage of the snapping technique is that the thin-film LCLV layers can be deposited on the whole wafer before dicing. This greatly reduces the handling of individual dice and thereby also increases throughput and yield.

2. First Wire Bonding

This is the second area in which improvements have been made that significantly improve our throughput and yield. The next process after depositing the LCLV layers and dicing is the attachment of one end of a wire bond to the chip bonding pads. The other side (the read-out side) must face the outside world; thus, the chip wire bonding pads, which are on the back (the CCD side), must face towards the package (see Figure 34). This is inverted with respect to normal chip packaging. To accomplish this packaging we first attach one end of the wire-bond wire (1-mil-diameter gold wire) to the chip pads and then let the

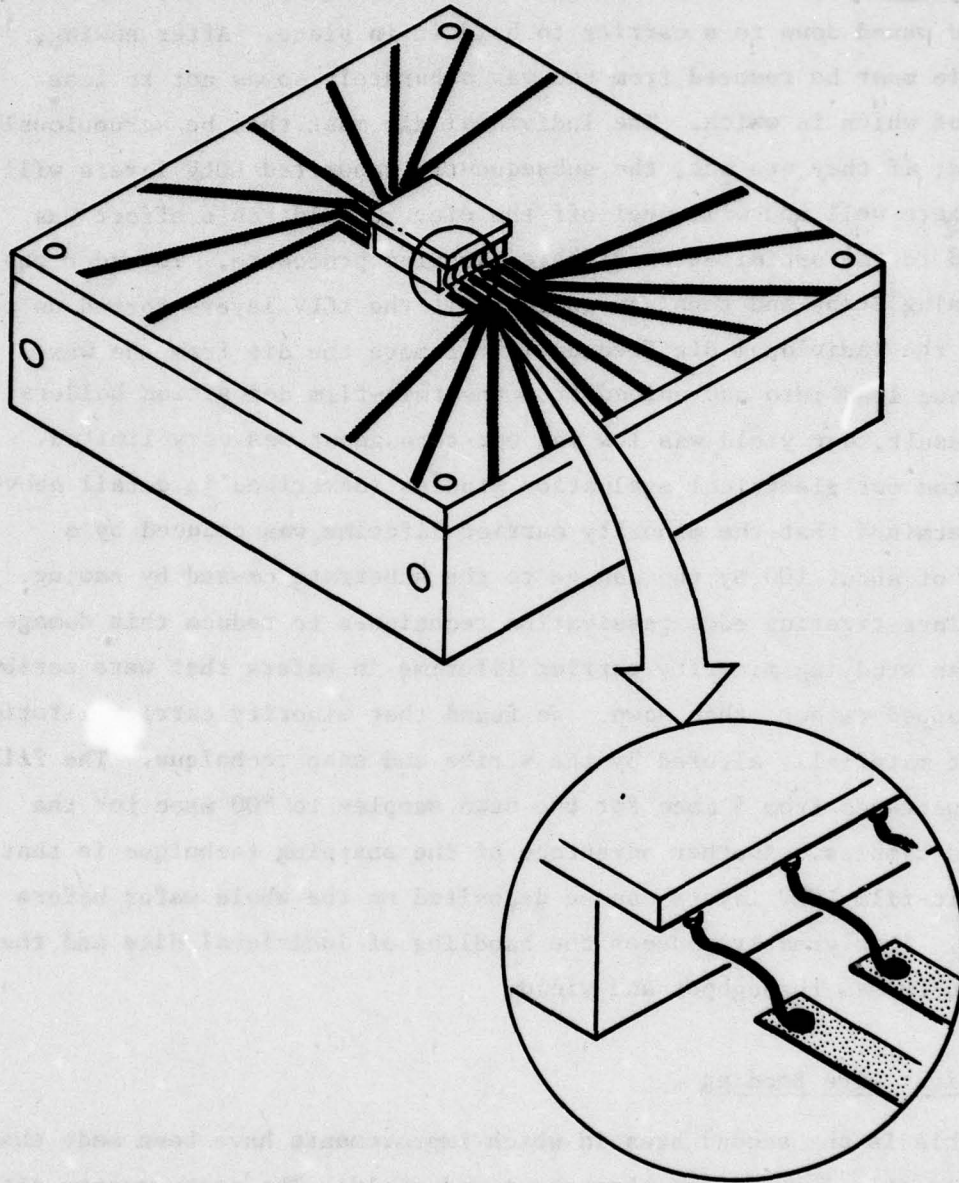


Figure 34. Schematic view of CCD LCLV chip mounted in partially assembled LV package.

other end dangle free. When wires have been bonded to each of the chip pads, the chip is inverted and the dangling ends are attached to the appropriate pads on the microstrip plate (Figure 34). Attaching the dangling ends — called second wire bonding — does not immediately follow the first wire bonding step. Before the second wire bonding step, the chip must be mounted on an intermediate support — a glass cube — to provide it with mechanical rigidity and optical flatness. This procedure will be described later, but suffice it to say that during the procedure the dangling ends of the wire bonds become quite tangled — so much so that while they are being untangled they often break. The delicate job of untangling these 1-mil-diameter gold wires substantially reduces our throughput and yield.

We have solved this problem, which is unique to this upside-down mounting geometry, by using a temporary wire bond storage frame (see Figure 35). Normal stitch wire bonds are made from the chip pads to the storage frame. Later, when the wire bonds are to be attached to the microstrip plate, the frame and the chip are inverted. Then the wires are cut loose at the storage frame and wedge bonded to the microstrip plate. The wire bond storage frame is made of 5-mil-thick stainless steel that is gold plated for good adhesion of the wire bonds. This storage frame must be very light because the storage frame is suspended from and totally supported by the wire bonds while the mounted device is being installed into the package. The implementation of this novel idea has reduced the processing time and significantly improved our packaging yield (from 30% to 75%).

3. Die Mounting and Flattening

After the semiconductor processing, the thin silicon chips are neither flat nor rigid. A mounting technique (illustrated in Figure 35) has been devised that is compatible with the prior and subsequent processing. In this technique, the thin silicon chip is laid, read-out side down, on an optically flat quartz plate. An adhesive is placed

on the back (CCD) side. We have found it convenient to use a thin (0.005 in.) Mylar sheet that is coated on each side with a commercially available thermal-setting adhesive. To allow for adhesive overflow, the adhesive-coated Mylar is cut to be slightly smaller than the Pyrex support cube. The Pyrex support cube is then placed on top of the adhesive and the assembly is clamped tightly together. The clamped assembly is then placed in an oven to activate the adhesive.

The long-term utility of the CCD LCLV as an advanced spatial modulator depends on the optical quality of the device. Thus, conflicts arose in the packaging between electrical and optical requirements. These conflicts were resolved with novel and innovative solutions that achieve the requirements for optical quality and electrical performance.

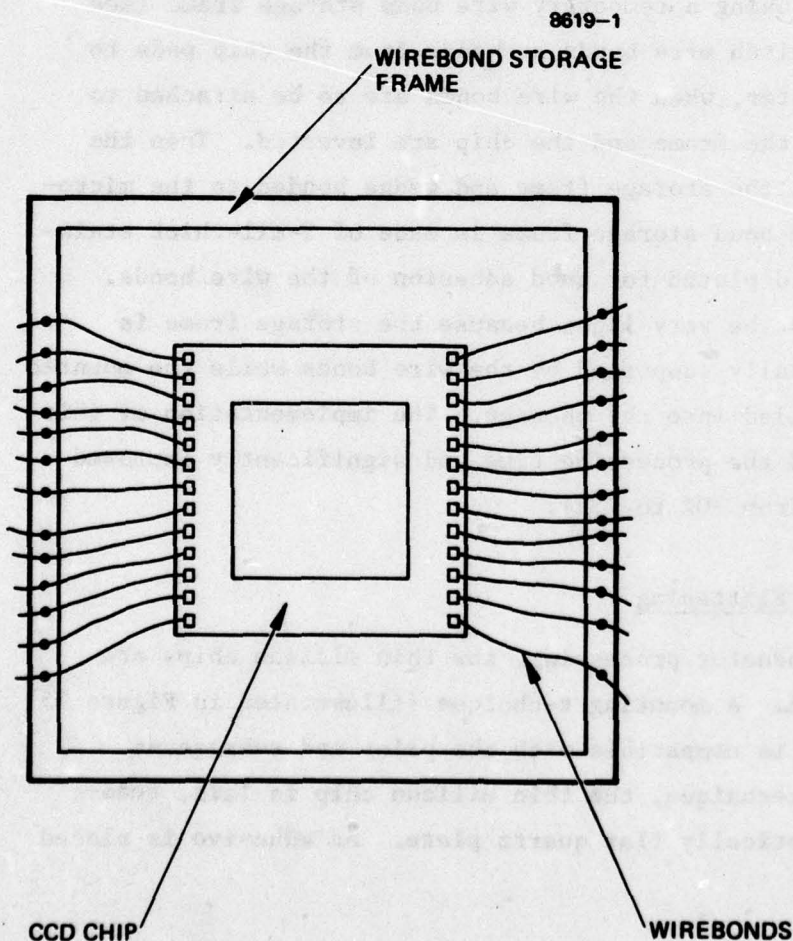


Figure 35.
Wire bond storage
frame with the wire
bonds in place.

The basic difficulty in obtaining a high-optical-quality device is the thinness of the CCD die. It is very desirable for electrical reasons (low-voltage operation, low dark current, and high resolution) to have as thin a silicon chip as possible; however, this conflicts directly with optical considerations. With a thin substrate, the CCD LCLV chip is susceptible to mechanical deformation by the high-temperature semiconductor processing and by the subsequent deposition of the LCLV layers on the read-out side. Our approach to achieving the stated optical flatness goal is the result of experience gained on two other LC projects where a silicon wafer was used as the optical substrate: a MOS matrix/LC display device and the silicon photoactivated LCLV. In both of these devices, the reflective layer deposited on the silicon wafer had to serve in the completed device as a very flat optical component. Since the MOS matrix/LCLV device operates with incoherent white light, the flatness requirements are not as stringent as for a coherent optical data processing element such as the CCD LCLV. A typical flatness that we have achieved in the mounted MOS matrix/LC device is 5λ across the 6-cm aperture. This would scale to $\lambda/6$ for the smaller CCD LCLV device.

As mentioned above, the main causes of distortion of the silicon CCD substrate are the high-temperature semiconductor processing and the deposition of the LBL and DM. Before semiconductor processing, 2-in.-diameter silicon wafers typically exhibit 2 or 3 hill and valley cycles with a peak-to-peak amplitude of ~ 20 visible fringes. After processing, the number of hill and valley cycles has increased to 4 or 5 while the depth of these distortions has increased to ~ 30 fringes peak to peak. The additional distortions are believed to be due to the nonuniform distribution of thermally grown oxides, diffusions, deposited polysilicon, etc. The second main cause of wafer distortion, the vacuum-deposited LCLV layers, are troublesome because they are highly strained layers. These thin films are deposited at elevated temperatures, typically 200°C for the LBL and 400°C for the DM. As the wafers are returned to room temperature after the depositions, the films and the silicon wafer are stressed because of mismatches in the thermal expansion coefficients.

Briefly, the technique we have developed to reduce these wafer distortions is to clamp the individual CCD dice against an optically flat surface (Figure 36), which must have an optical figure as good as or better than the desired optical figure of the CCD die. In effect, we mechanically deform the semi-flexible silicon chip and thereby replicate the optical figure of the clamping plate. It was necessary to modify this technique to accommodate the small size of the CCD chips before we could begin evaluating the technique experimentally. We subsequently have performed some preliminary evaluations. On dummy chips the same size as the CCD die that had no circuits but did have the thin-film LCLV layers, we were able to achieve an optical figure of $\sim 1/4$ of one fringe across the central 60% of the die, which is somewhat larger than the active area of the CCD die. Thus, with these dummy silicon dice, we have been able to demonstrate an optical figure of better than $\lambda/10$. The best optical figures we have been able to achieve to date on test CCD LCLV chips are not this good because there is some risk of breaking the die with this flattening operation and there are several other key CCD LCLV issues to be resolved. The flattening technique involves squeezing the CCD LCLV substrate between two rigid members: the support structure and the optically flat plate. Our yield when flattening the dummy dice was about 75%. Since we had data from these experiments with dummy dice that indicated that flattening chips to a high optical figure was possible but we had no data regarding the optical performance of these first CCD LCLVs, we chose not to pursue the flattening issue at that time. The result is that the best optical figure we have obtained with relaxed flattening pressures is $\lambda/2$. Another contributing factor to this decision was the complexity of the CCD LCLV assembly.

After having successfully demonstrated some of the key issues regarding the CCD LCLV technology, we feel that it is now appropriate to address the question of optical figure in fully processed CCD LCLVs.

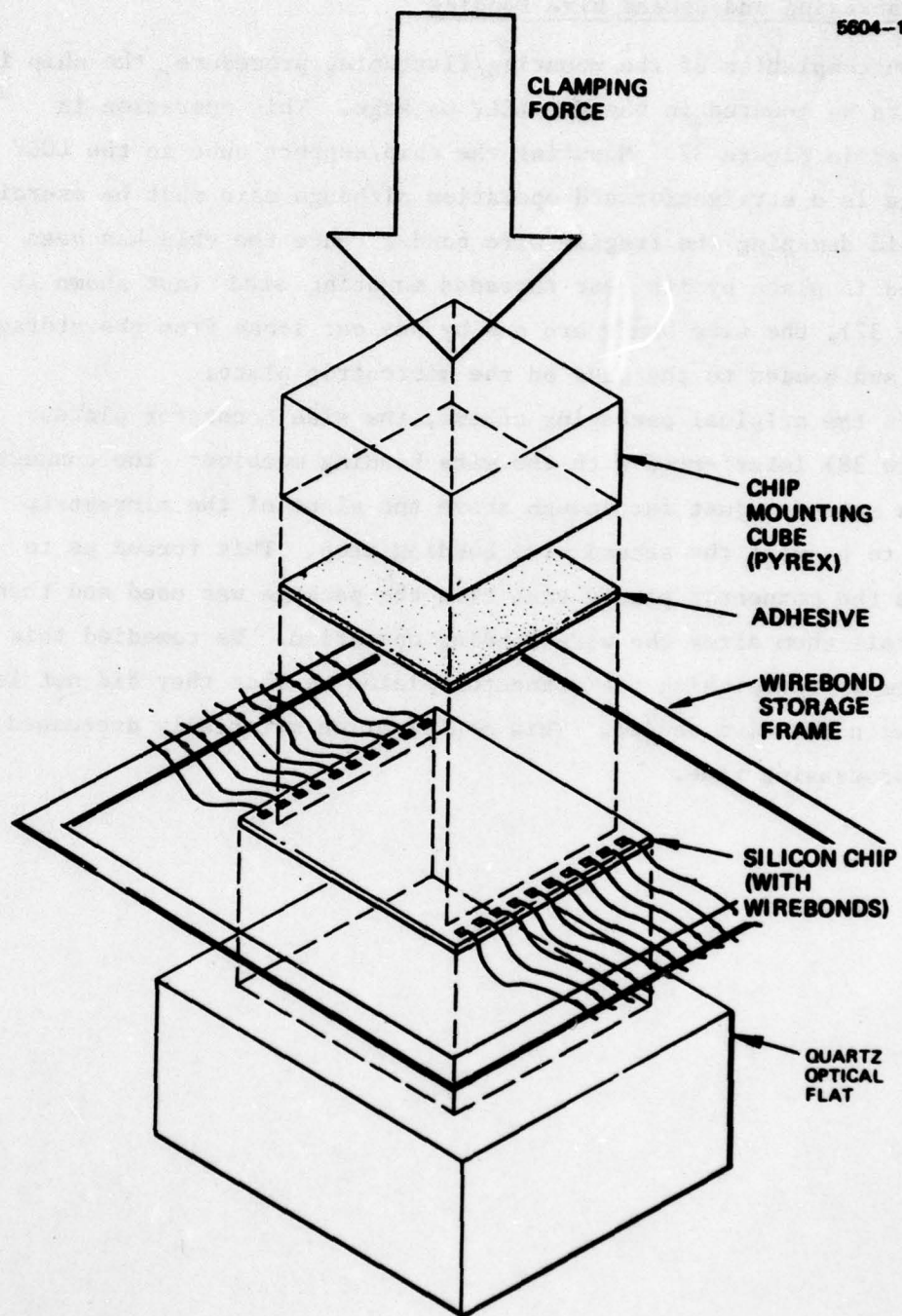


Figure 36. Schematic view of chip-mounting/flattening technique.

4. Packaging and Second Wire Bonding

On completion of the mounting/flattening procedure, the chip is ready to be mounted in the CCD LCLV package. This operation is depicted in Figure 37. Mounting the chip/support cube in the LCLV package is a straightforward operation although care must be exercised to avoid damaging the fragile wire bonds. Once the chip has been secured in place by its rear threaded mounting stud (not shown in Figure 37), the wire bonds are one by one cut loose from the storage frame and bonded to the pads on the microstrip plate.

In the original packaging scheme, the side connector plates (Figure 38) interfered with the wire bonding machine: the connector plates extended just far enough above the plane of the microstrip plate to prevent the second wire bonding step. This forced us to remove the connector plates each time the package was used and then reinstall them after the wire bonding operation. We remedied this problem by redesigning the connector plates so that they did not interfere with the wire bonder. This modification materially decreased our LCLV processing time.

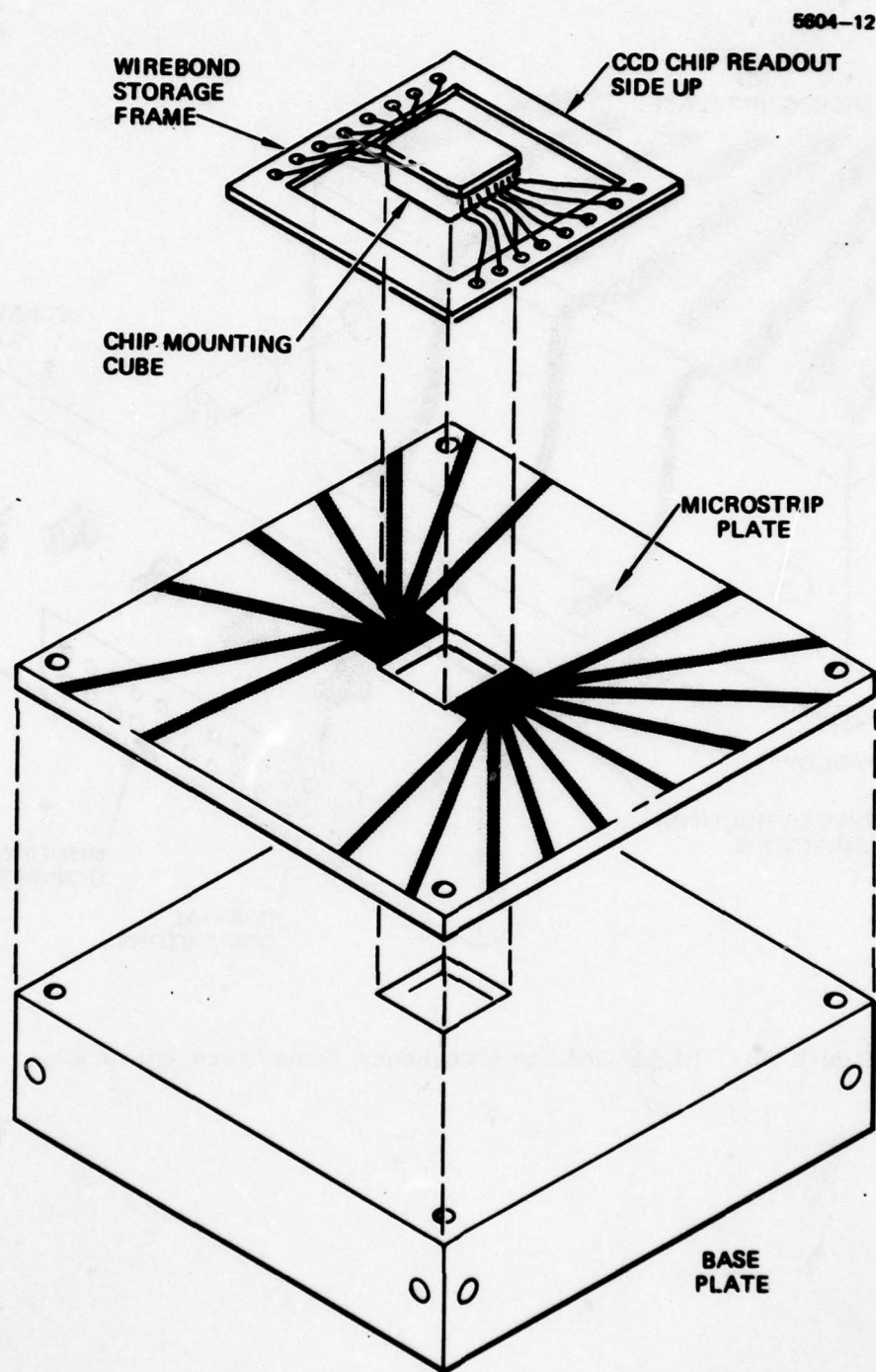


Figure 37. Mounting supported CCD LCLV chip onto the base plate.

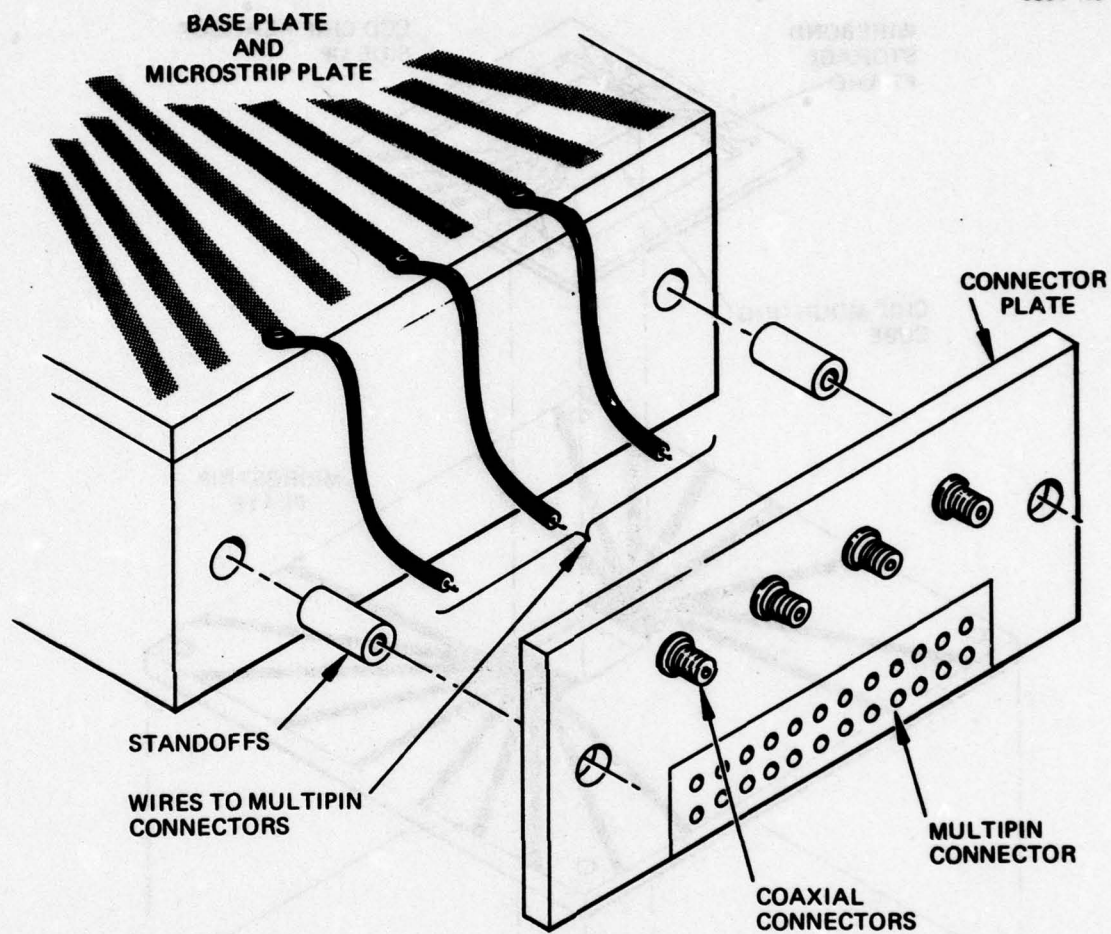


Figure 38. High- and low-frequency connectors emplaced.

5. Final Assembly of the CCD LCLV

Just before the final assembly of the LCLV, a thin-film vacuum deposition of SiO_x is done to provide a surface-alignment layer for the LCLV. The CCD LCLV package with the CCD chip mounted in place is suspended in the vacuum evaporator such that the SiO_x evaporant impinges on the surface of the CCD chip at grazing incidence. The LCLV package is shielded from the evaporant with a shadow mask. This very thin layer of SiO_x (typically 50 Å) deposited in this way causes the LCLV molecules to align with their long axis parallel to the plane of the surface of the CCD chip.

With the aid of a low-power microscope and in a clean area (laminar flow bench), a drop of LCLV is placed on the readout surface of the CCD chip. The counterelectrode plate assembly is then lowered into place (the surface of the counterelectrode having previously been treated for LCLV alignment in a manner similar to the way the CCD chip had been). During this final assembly step, the counterelectrode must be carefully aligned with the display area on the chip before the two surfaces are actually mated (Figure 39). To ensure uniform LCLV thickness, the counterelectrode must be forced down onto the CCD chip until the perimeter SiO_x spacers touch the surface of the CCD chip. If the counterelectrode is misaligned with respect to the CCD chip, the SiO_x spacer will press on the unsupported portion of the CCD chip and fracture it. Provisions for lateral and rotational adjustment have been incorporated into the design of the counterelectrode top plate assembly (Figure 40). Final tuning of the LCLV thickness is done using optical techniques to determine the proper final adjustment of the clamping screws. A photograph of an assembled CCD LCLV is shown in Figure 41.

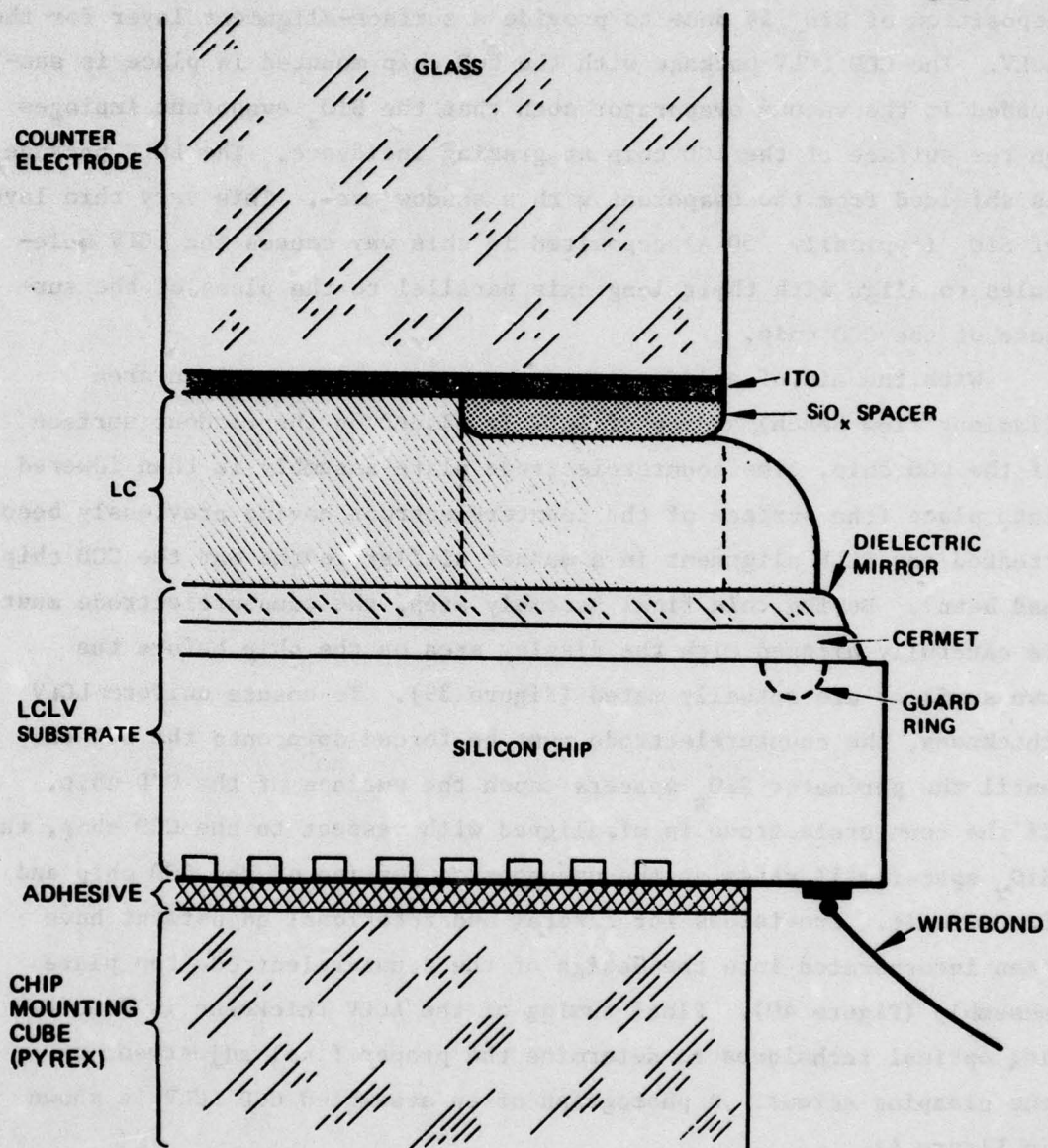


Figure 39. Relationship between the counterelectrode and the CCD chip during final assembly in the LCLV.

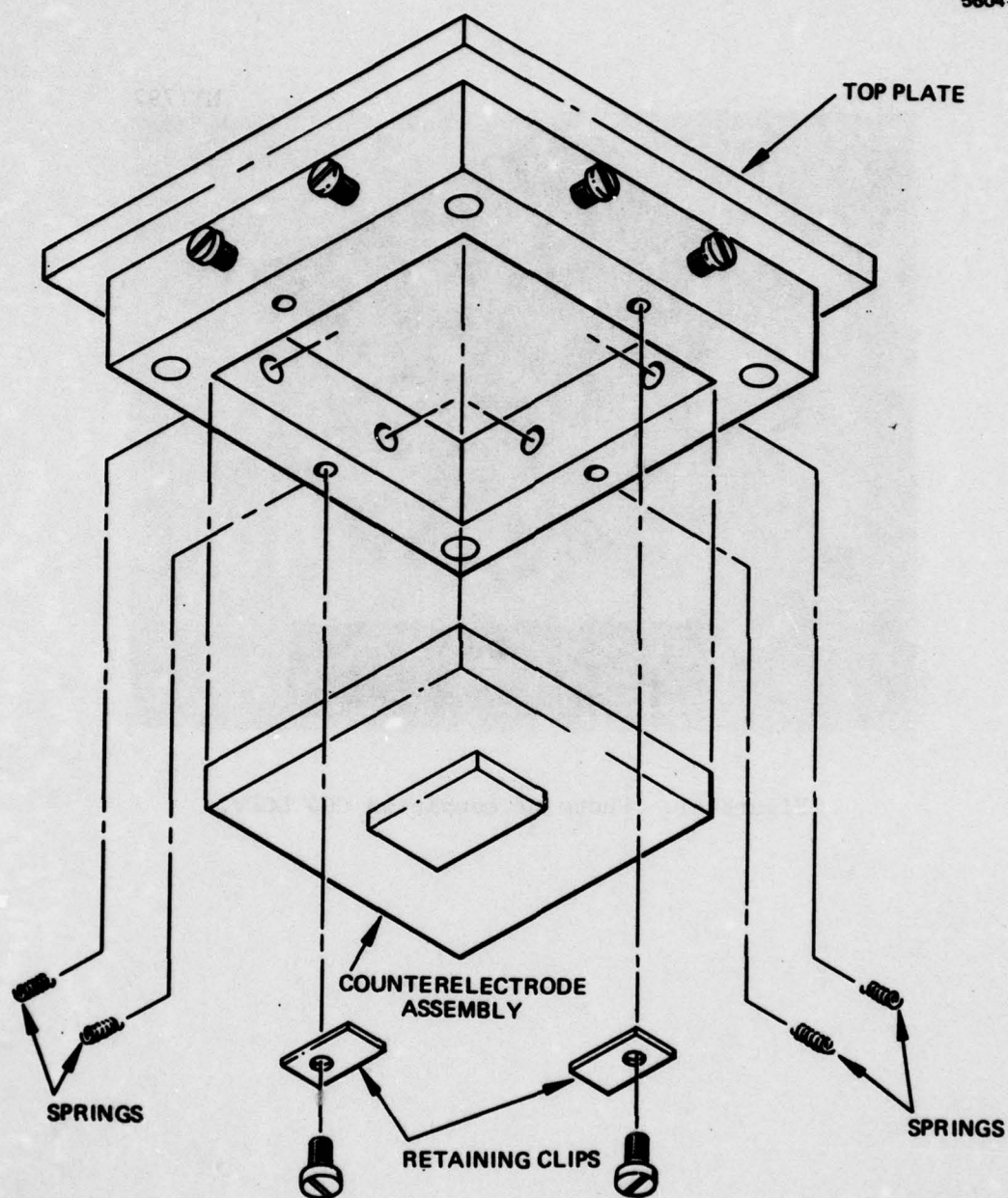


Figure 40. CCD LCLV top plate assembly.

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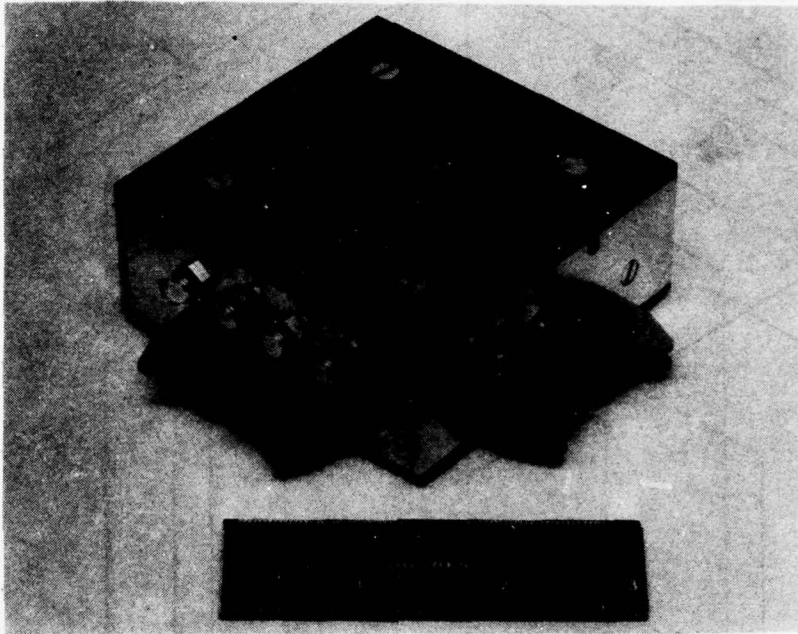


Figure 41. Photo of completed CCD LCLV.

SECTION 6

CONCLUSIONS

The overall objectives of this program were the continued development of the CCD LCLV. Specific targets within this framework were:

- To demonstrate the performance level of the buried-channel-to-surface-channel CCD transfer.
- To demonstrate the capability of serially inputting an image pattern into the serial CCD register, then transferring it to the parallel array, and finally transferring the spatial pattern to the readout LC side.
- To demonstrate the overall implementation of the above by fabricating a fully operational CCD LCLV.

The buried-channel-to-surface-channel transfer has been successfully demonstrated with a transfer efficiency of over 95%. Surface-channel CCD performance was demonstrated both by the successful operation of the serial-to-parallel transfer and by achieving a surface-channel transfer efficiency of 0.9998. Finally, a fully operational CCD LCLV was fabricated showing a spatial resolution of 12 lines and a maximum contrast ratio of 50:1.

In addition to the above, the following achievements were realized:

- An improved chip dicing method resulting in an increased fill time from 5 to 500 msec.
- An improvement in packaging which resulted in an increase in final device yield from 30% to 80%.
- The assessment of several alternative input-loading schemes on the SCCD serial input register for improved analog-signal linearity.
- The determination of the effect of the Si/SiO₂ interface states on the serial transfer efficiency.
- Resolution capabilities up to the microgrid linewidth have been demonstrated on the photoactivated device, thus demonstrating the capability to achieve the ultimate resolution goal of the CCD device.

In the next phase of this program, we recommend that the main effort be invested in further investigating and improving:

- (1) The transfer mechanism from the CCD parallel array to the readout side.
- (2) The structure and fabrication procedures of the MOS readout structures.

Specifically in (1), epitaxial layer resistivity and thickness should be optimized. In (2), achievements on the photoactivated device such as the implementation of the Si/SiO₂ dielectric mirror, the novel n- π microgrid structure, and the improvements achieved by an annealing process following thin film deposition, should be implemented in the CCD readout structure.

Further studies are recommended in the following areas:

- The degradation caused to the MOS structure by thin-film deposition.
- The edge breakdown effect observed in the photoactivated device.
- Substrate resistivity and minority carrier lifetime degradation due to the many high-temperature semiconductor processes involved.
- Improved optical flatness by the reduction of process-induced wafer distortions and the utilization of corrective mounting techniques.

Since 100-MHz input rates can be achieved with current buried-channel CCD technology, we recommend that the effort toward implementing this goal should be deferred.

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